

Quarterly Technical Report

Solid State Research

2004:1

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS



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**Massachusetts Institute of Technology
Lincoln Laboratory**

Solid State Research

**Quarterly Technical Report
2004:1**

1 November 2003 – 31 January 2004

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 November 2003 through 31 January 2004. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

Values of thermo-optic properties of AgGaSe_2 , a nonlinear material for the infrared, have been measured as a function of temperature from ~ 300 to 100 K. The average power handling of the nonlinear conversion crystal is expected to improve at cryogenic temperatures.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

A nearly circular, single spatial mode with cw output power up to 1 W has been demonstrated from a 915-nm slab-coupled optical waveguide laser. Beam quality measurements indicate that the output is nearly diffraction limited in both the horizontal and vertical directions.

3. SUBMICROMETER TECHNOLOGY

A high-speed thermally activated optical switch, operating at 1.55- μm wavelength, has been developed using silicon micromachining techniques. Submicrosecond switching times have been demonstrated with silicon optical waveguides that are directly heated by an electric current.

A low-loss optical waveguide structure has been developed that combines multimode and single-mode silicon waveguides in a serpentine layout. The single-mode waveguides prevent the excitation of higher-order modes in the turns, while the straight multimode sections reduce scattering loss, to achieve an overall loss of 0.32 dB/cm in meter-long structures.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

The compatibility of the CANARY (Cellular Analysis and Notification of Antigen Risks and Yields) assay with food samples has been established. Simple, rapid sample preparation techniques have been developed that reduce the effect of inhibitors present in three food types.

5. ADVANCED IMAGING TECHNOLOGY

Diode arrays incorporating the fully depleted silicon-on-insulator complementary metal-oxide semiconductor backend-metal process that are fully compatible with three-dimensional wafer integration techniques have been fabricated. The measured dark currents for these arrays containing 8-, 16- and 24- μm -pixel diodes were similar to or lower than our previous low-dark-current diode arrays fabricated using conventional wet-etch processing techniques.

6. ANALOG DEVICE TECHNOLOGY

A fully depleted silicon-on-insulator charge-coupled device (CCD) has been demonstrated. A new process was developed that allows the array of CCD gates to be fabricated within a single layer of polycrystalline silicon (polysilicon), which produces well-controlled, very narrow gaps in a polysilicon layer.

7. ADVANCED SILICON TECHNOLOGY

Microelectromechanical series capacitive switch technology has been modified and enhanced to produce analog, multi-state, and multi-bit varactors for application in tunable filters, matching networks, and oscillators. An analog varactor with nearly 7:1 usable tuning range and better than 80:1 switching range, a multi-state varactor switch, and a 4-bit capacitor bank have been demonstrated.

REPORTS ON SOLID STATE RESEARCH

1 NOVEMBER 2003 THROUGH 31 JANUARY 2004

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Simulation Study of Process Latitude for Liquid Immersion Lithography	S.-Y. Baek* D. C. Cole* M. Rothschild M. Switkes M. S. Yeung* E. Barouch*	<i>J. Microlith., Microfab., Microsyst.</i> 3 , 52 (2004)
Morphology Evolution and Luminescence Properties of Porous GaN Generated via Pt-Assisted Electroless Etching of Hydride Vapor Phase Epitaxy GaN on Sapphire	D. J. Diaz* T. L. Williamson* I. Adelida* P. W. Bohn* R. J. Molnar	<i>J. Appl. Phys.</i> 94 , 7526 (2003)
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*Author not at Lincoln Laboratory.

Widely Tunable, Aluminum-Free,
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Semiconductor Lasers

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Effect of Dislocations on Local
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Low Polarization Dependent
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Pump-Induced Bleaching of the
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Nd:YAG/Cr⁴⁺:YAG Passively
Q-Switched Microchip Lasers

J. J. Zayhowski
A. L. Wilson, Jr.

IEEE J. Quantum Electron.
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Design and Process Integration of
an Electric Induction Micromotor

C. Livermore*
J. Yoon
T. Lyszczarz

50th American Vacuum Society
International Symposium,
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2-7 November 2003

AlGa_N Materials Development for
UV Emitters

R. J. Molnar
J. Caissie
J. W. Caunt
R. Slattery
G. W. Turner

Semiconductor Ultraviolet
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Program Review,
Austin, Texas,
18 November 2003

Optical Lithography and the End of
the Semiconductor Roadmap

M. Rothschild

MIT/Lincoln Laboratory
Seminar Series on
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Lexington, Massachusetts,
19 November 2003

Quantum-Dot Superlattice Power
Generator Multi-couple Arrays for
Waste Heat Conversion

T. C. Harman
R. E. Reeder
M. P. Walsh
B. E. LaForge

Fall Meeting of the Materials
Research Society,
Boston, Massachusetts,
1-5 December 2003

Temperature Dependence of
Intermodulation Distortion in
YBCO (Intrinsic or Extrinsic?)

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Fall Meeting of the Materials
Research Society,
Boston, Massachusetts,
1-5 December 2003

Non-contact Determination of
Free Carrier Concentration in
n-GaInAsSb

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Fall Meeting of the Materials
Research Society,
Boston, Massachusetts,
1-5 December 2003

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[†] Titles of presentations are listed for information only. No copies are available for distribution.

Self-Organized Superlattices in GaInAsSb Grown on Vicinal Substrates	C. A. Wang C. J. Vineis* D. R. Calawa	Fall Meeting of the Materials Research Society, Boston, Massachusetts, 1-5 December 2003
CANARY B-Cell Sensor for Rapid Sensitive Identification of Pathogens	M. A. Hollis	4th International Detection Technologies Conference, Arlington, Virginia, 8-9 December 2003
High Speed Sub-25-nm Schottky Barrier <i>p</i> MOS	M. Fritze C. Keast P. Wyatt C. L. Chen	IEEE International Electron Devices Meeting, Washington, D.C., 8-10 December 2003
Mechanism for Intersublattice Magneto-optical Pair Transitions in Ferrimagnetic Garnets	G. Dionne G. A. Allen*	9th Joint Magnetism and Magnetic Materials–Intermag Conference, Anaheim, California, 5-9 January 2004
Magnetic Domain Control of Microwave Ferrite Resonators	G. Dionne D. Oates	9th Joint Magnetism and Magnetic Materials–Intermag Conference, Anaheim, California, 5-9 January 2004
Challenges for Modeling and Fabrication of Robust RF MEMS	J. B. Muldavin	Technical Presentation, Meeting of Boston Chapter of IEEE, Lexington, Massachusetts, 14 January 2004
Fabrication of DAST Electro-optic Waveguides Using Graphoepitaxial Crystal Growth	M. W. Geis	Lincoln Laboratory Technical Seminar Series, Massachusetts Institute of Technology, Cambridge, Massachusetts, 21 January 2004

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Three-Dimensional Imaging with
Arrays of Geiger-Mode Avalanche
Photodiodes

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SPIE Photonics West,
San Jose, California,
24-29 January 2004

Prospects for 157-nm Liquid
Immersion

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International SEMATECH
Immersion Lithography
Workshop,
Los Angeles, California,
26-27 January 2004

Water for Immersion Lithography

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International SEMATECH
Immersion Lithography
Workshop,
Los Angeles, California,
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Mobile Surface Electrons on
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ADVANCED SILICON TECHNOLOGY

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1. QUANTUM ELECTRONICS

1.1 MEASUREMENT OF THERMO-OPTIC PROPERTIES OF AgGaSe₂ IN THE TEMPERATURE RANGE FROM ~300 TO 100 K

AgGaSe₂ is a uniaxial crystal with a room-temperature bandgap of 1.689 eV (734 nm) for the polarization parallel to the c-axis, and 1.713 eV (724 nm) for the polarization parallel to the a-axis. The c- and a-axes are parallel and perpendicular to the axis of uniaxial symmetry. AgGaSe₂ is an attractive nonlinear material for applications involving frequency conversion such as second harmonic generation [1],[2] and parametric conversion [3] in the infrared region from ~1 to 15 μm . The average power handling of the nonlinear conversion crystal is expected to improve at cryogenic temperatures, because of better values of the thermo-optic properties at lower temperatures. We have measured values of thermal diffusivity β , specific heat C_p , thermal conductivity κ , coefficient of thermal expansion α , and dn/dT in the temperature range from ~300 to 100 K. Larger values of β and κ , and smaller values of α and dn/dT are desirable for improved performance of the nonlinear material.

β and C_p were measured at NETZSCH (Burlington, Mass.) with a laser flash technique [4] utilizing a Holometrix Thermoflash 2200 instrument (ASTM Standard E1461-01). Measurements were made on disks 12.7 mm in diameter and 3.1 mm thick with thickness along the a- and c-axes. κ is obtained from β and C_p using the relationship

$$\kappa = \beta C_p \rho \quad (1.1)$$

where ρ is the density of the crystal. Thus, κ was deduced from the measured values of β , C_p , and ρ . Measured values of β and deduced values κ for the a- and c-axes are plotted in Figure 1-1 as a function of temperature. The accuracy of the κ values was estimated to be $\pm 7\%$. Our values of 0.95 and 1.03 W/m·K at 298 K for κ along the c- and a-axes, respectively, are in agreement with the corresponding values of 1.0 and 1.1 W/m·K reported previously [5]. As expected, values of both β and κ increase with decrease in temperature. Higher values of β and κ are desirable because the increase in the temperature of the nonlinear crystal due to the power absorbed from the incident laser radiation is lower for higher values of β and κ .

Thermal expansion was measured at PMIC (Corvallis, Ore.) using a double Michelson laser interferometer (ASTM Standard E289-95). Measurements were made on 3.1-mm-diameter rods with a length of 25.4 mm along the c- and a-axes. α was deduced from the measured thermal expansion over a temperature interval ΔT of 10 K. Values of α for the a- and c-axes, deduced in this manner, are plotted in Figure 1-2. Note that the values of α along the c-axis are negative. Our results are generally consistent with those of Bodnar and Orlova [6], obtained from X-ray measurements as a function of temperature.

Values of dn_o/dT and dn_e/dT were obtained from the frequency shift with temperature of the fringes in the Fourier transform infrared (FTIR) transmission spectra for the polarizations along the a- and c-axes,

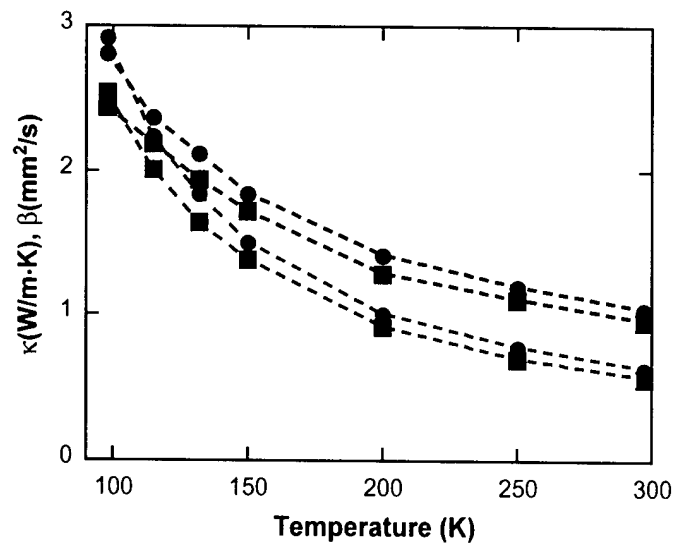


Figure 1-1. Measured values of thermal diffusivity β and thermal conductivity κ of AgGaSe_2 along the a - and c -axes in the temperature range from 298 to 95 K. The circles and squares represent the data for the a - and c -axes, respectively.

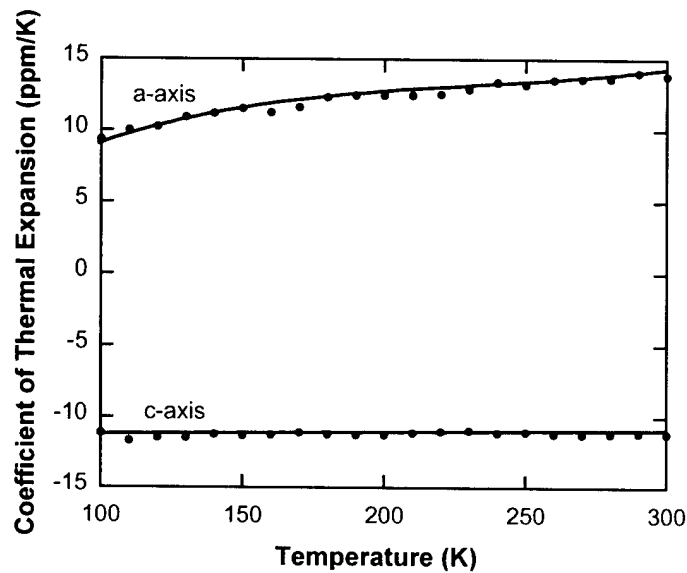


Figure 1-2. Measured values of the coefficient of thermal expansion α of AgGaSe_2 along the a - and c -axes in the temperature range from 300 to 100 K. The circles represent the data points, and the curves are the third-order polynomial and linear fits to the a - and c -axes data, respectively.

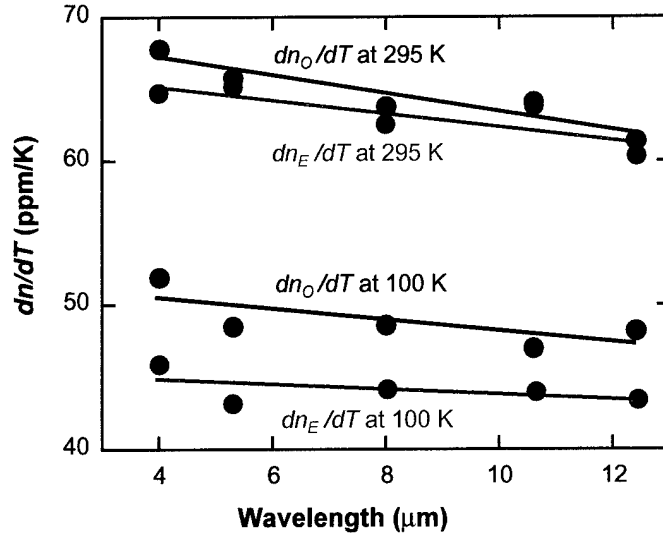


Figure 1-3. Measured values of dn_O/dT and dn_E/dT of $AgGaSe_2$ at 295 and 100 K in the spectral range from 4.0 to 12.4 μm . The circles represent the data, and the curves are the linear fits to the data.

respectively. A 2.025-mm-thick etalon with thickness along the a-axis was used for these measurements. The FTIR spectra were obtained using a Nicolet FTIR spectrometer model Protégé 460 with a spectral resolution of 0.5 cm^{-1} . The subscripts O and E of n are for the ordinary and extra-ordinary rays, respectively, corresponding to the polarizations along the a- and c-axes. The relationship between dn/dT and the frequency shift $\Delta\nu$ for a temperature increase ΔT is given by

$$\frac{dn}{dT} = -\left(\frac{n}{\nu}\right)\left(\frac{\Delta\nu}{\Delta T}\right) - n\alpha \quad (1.2)$$

where n is the value of the refractive index and ν is the frequency of the fringe. The values of dn_O/dT and dn_E/dT are plotted in Figure 1-3 as a function of wavelength from 4.0 to 12.4 μm for temperatures of 295 and 100 K. We note that both dn_O/dT and dn_E/dT decrease somewhat with increase in wavelength. In contrast, Tanaka and Kato [7] have reported a small increase in dn_O/dT and dn_E/dT with increase in wavelength at room temperature. Also, we find that dn_O/dT is somewhat larger than dn_E/dT . Again, our result is opposite to that of [7]. Furthermore, our values of dn_O/dT and dn_E/dT at 295 K are lower than the room-temperature values of [7], and those of Bhar et al. [8] obtained for the temperature range from 293 to 573 K.

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 HIGH-POWER, NEAR DIFFRACTION-LIMITED AlGaAs-InGaAs SEMICONDUCTOR SLAB-COUPLED OPTICAL WAVEGUIDE LASER

Single-mode, diffraction-limited semiconductor diode lasers with output power in the 1-W range are of interest for a variety of applications, including free-space optical communications and pumping ytterbium- and erbium-doped single-mode optical fibers. For ytterbium-doped silica fiber lasers, strong absorption occurs in two wavelength regimes, 975 and 915 nm [1], so that high-power, single-mode pumps emitting at both wavelengths are of interest. Furthermore, beam quality, brightness, and aspect ratio are important considerations for pump lasers. Conventional monolithic high-power semiconductor diode lasers usually have highly elliptical mode profiles [2], which require external optics or lensed fibers for efficient fiber coupling. A near diffraction-limited circular beam has been demonstrated in a >0.5-W vertical cavity semiconductor laser structure using an external cavity and optical pumping [3], but this approach is more complicated than that of a monolithic diode structure.

Recently, we proposed and demonstrated a new class of semiconductor diode laser, the slab-coupled optical waveguide laser (SCOWL). This new class of devices utilizes slab coupling of higher-order modes to achieve lasing in a single spatial mode. Because the fundamental SCOWL mode results from a slab-coupled rib waveguide [4], it is possible to design the waveguide so that the relatively large output mode is near diffraction-limited and nearly circular in aspect ratio. SCOWL devices have been demonstrated in three wavelength regimes: 1.3 μm [5], 980 nm [6], and 915 nm [6]. Here, we describe the extension of the 915-nm devices to the 1-W output power level [7]. We also report on beam quality measurements on these devices, including characterization of M^2 of the beam output. These measurements show that near diffraction-limited performance is achieved in SCOWL devices.

A schematic, cross-sectional diagram of the 915-nm SCOWL devices reported here is shown in Figure 2-1. This structure is similar to that described previously [6]. The thickness of the waveguide layer is much larger than that used in standard single-mode lasers, and the height and width of the rib region are larger and nearly equal. In the order of the growth sequence, on a (100) n^+ -GaAs substrate, the design consists of a 1.0- μm -thick $2 \times 10^{18} \text{ cm}^{-3}$ GaAs buffer layer; a compositionally graded 0.1- μm -thick $1 \times 10^{18} \text{ cm}^{-3}$ n -AlGaAs layer; a 1.7- μm -thick n -Al_{0.30}Ga_{0.70}As lower cladding; a 3.9- μm -thick n -Al_{0.25}Ga_{0.75}As waveguide, in which the doping is about $1 \times 10^{17} \text{ cm}^{-3}$; the multiple quantum-well (MQW) gain region; a 1.6- μm -thick p -Al_{0.30}Ga_{0.70}As top cladding; a compositionally graded 0.1- μm -thick $1 \times 10^{18} \text{ cm}^{-3}$ p -AlGaAs layer; and a 100-nm-thick p^+ -GaAs contact layer. The nominally undoped MQW gain region consists of three 7-nm-thick In_{0.11}Ga_{0.89}As quantum wells with ~0.8% compressive strain and two 10-nm-thick Al_{0.1}Ga_{0.9}As barrier and 6-nm-thick Al_{0.1}Ga_{0.9}As bounding layers. The thickness of the bounding layers was chosen to provide the desired confinement factor for the SCOWL mode. The transverse confinement factor Γ of the lowest-order slab mode is ~0.005; the lateral confinement in etched SCOWL devices reduces the overall confinement factor to ~0.003. Several

higher-order slab modes have transverse confinement factors 2–3 times higher and would potentially lase first if not filtered out in the etched SCOWL by the slab.

Devices are fabricated using bromine ion-beam-assisted (Br-IBAE) dry etching, followed by a short chemical wet etch to define the rib structure. An Al_2O_3 etch mask is used for the Br-IBAE etching, which is performed with the wafer at 40°C . The etched areas (grooves in Figure 2-1) were chosen to be $30\text{ }\mu\text{m}$ wide. After etching, the wafer is coated with SiO_2 , contact openings are made on the rib, and the entire top surface is metallized. The wafer is then thinned to about $100\text{ }\mu\text{m}$, and a back ohmic contact is applied.

Device bars are then cleaved to length, and a passivation coating consisting of a $25\text{-}\text{\AA}$ -thick layer of gadolinium and a $200\text{-}\text{\AA}$ -thick layer of gadolinium-gallium-garnet is deposited on each facet [8]. Over the passivation coatings, a nominal 95% coating is deposited on the back facet, and a 5% reflectivity coating is deposited on the output facet. Individual devices are then mounted junction side down onto a copper heatsink using indium solder. Wire bonds are made to the back of the device, and the heatsink is mounted on a thermoelectric cooler (TEC).

The rib width and etch depth of a 1-cm-long device were designed to obtain a nearly circular spatial mode: $t = 3.2\text{ }\mu\text{m}$ and $w = 4.6\text{ }\mu\text{m}$, where t and w are defined in Figure 2-1. These device dimensions were chosen by using a two-dimensional complex index mode solver, taking into account the gain and loss in the different regions of the entire device structure. The resulting mode was nearly circular, with $3.8\text{-}\mu\text{m}$ (horizontal) by $3.4\text{-}\mu\text{m}$ (vertical) $1/e^2$ widths in the near field. The single-ended cw output power vs current of this 1-cm-long, 915-nm device is shown in Figure 2-2. The threshold, with the TEC set to 16°C , is

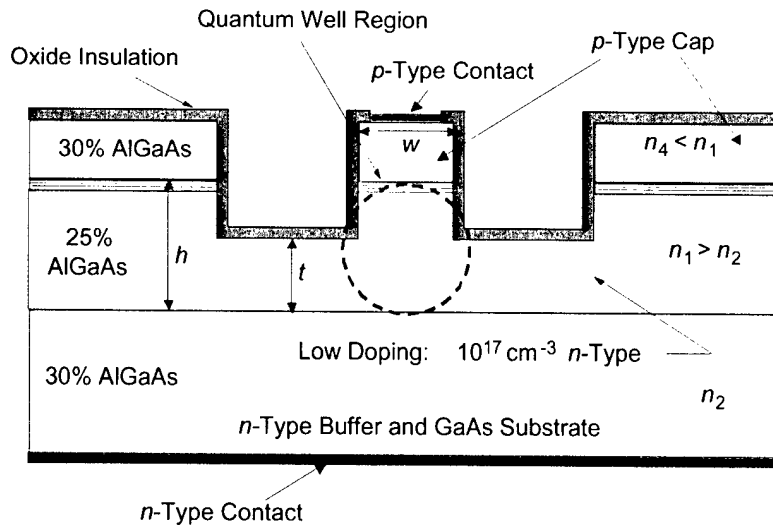


Figure 2-1. Cross-sectional diagram of 915-nm slab-coupled optical waveguide laser (SCOWL) structure.

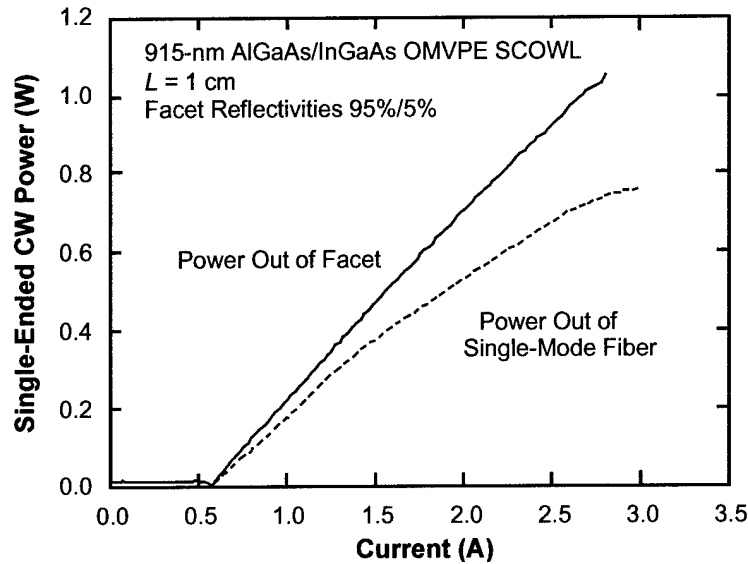


Figure 2-2. CW output power vs current of 1-cm-long 915-nm SCOWL with 95%/5% facet coatings. Power butt coupled into a single-mode fiber is also shown. The heatsink temperature was 16°C.

~0.55 A. The output power is about 1 W at 2.7 A. The power butt coupled (no lens) into an antireflection-coated single-mode fiber (4.2- μ m mode diameter) is also shown in Figure 2-3. At <2-A device current, >80% of the power from the laser facet is coupled into the fiber. At >2-A current, however, this butt-coupling efficiency degrades to about 75%. Possible reasons for this degradation in coupling efficiency are slight changes in beam width, external feedback effects at higher power levels, or changes in the fiber alignment due to thermal load.

In order to characterize the beam quality, M^2 measurements were performed on the SCOWL output beam. The quantity M^2 , the beam quality parameter, is a measure of the number of times that a gaussian laser beam is diffraction limited. In general, $M^2 \geq 1$, and $M^2 = 1$ corresponds to a diffraction-limited beam. Inherent in the use of M^2 is the assumption that the beam is approximately gaussian. Since waveguide modes are in general not truly gaussian, output beams are usually, if anything, closer to diffraction limited than indicated by M^2 . In order to measure M^2 , both the near- and far-field mode profiles are measured on a charge-coupled device (CCD) camera. The near- and far-field profile $1/e^2$ widths are extracted by binning the CCD images through the center of the profile, and the binned sections are fit to gaussian functions. The near-field profile is measured by using a low-aberration lens to magnify the image of the near-field mode on the camera. The far-field profile is measured by using the lens to collimate the beam. The M^2 of the beam can be determined from the $1/e^2$ widths of these beam profiles since $M^2 = \pi \Theta D_0 / 4\lambda$, where Θ is the full $1/e^2$ far-field divergence angle, D_0 is the near-field $1/e^2$ waist diameter, and λ is the laser wavelength.

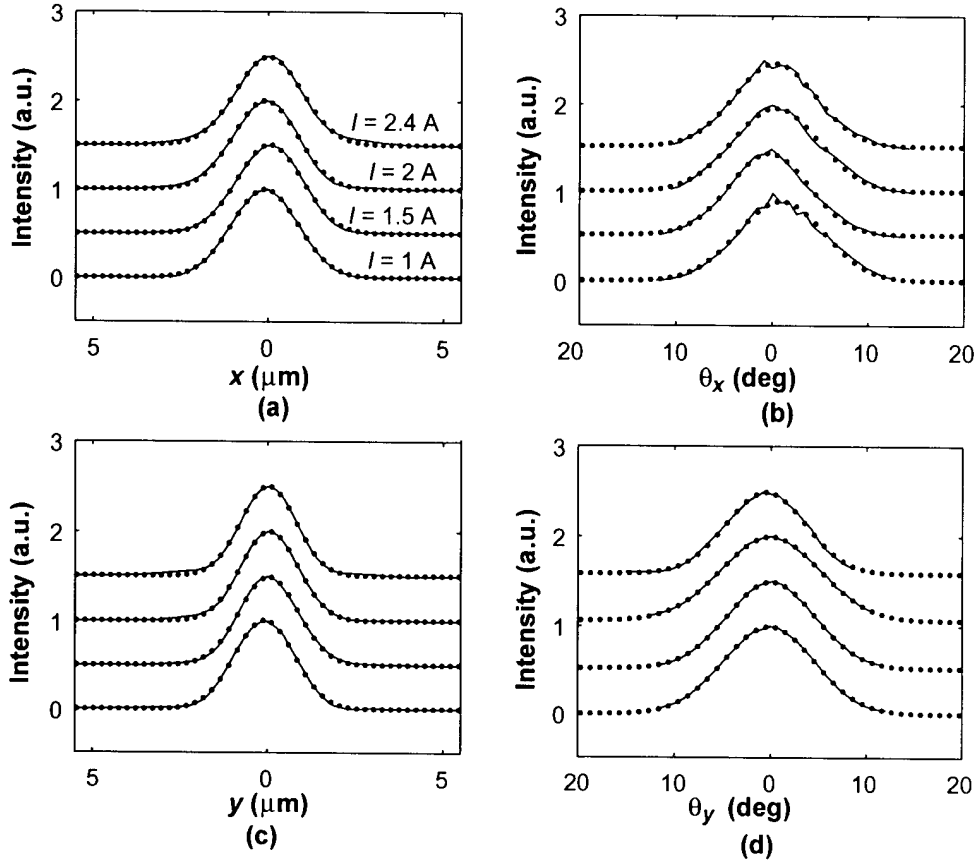


Figure 2-3. (a) Near-field and (b) far-field intensity slices through the x -direction (horizontal), and (c) near-field and (d) far-field intensity slices through the y -direction (vertical). Data are shown for increasing dc currents: 1, 1.5, 2, and 2.4 A. Solid curves show measurements, and dots show fits.

The measured and fitted near- and far-field profiles in both the x and y directions as a function of cw current are shown in Figure 2-3. These plots show that the data (solid curves) fit fairly well to gaussian profiles (fits shown by dots), indicating the above values for M^2 are a good measure of the quality of the output beam. By extracting the $1/e^2$ widths of the near- and far-field profiles, we obtain $M_x^2 \sim 1.1$ and $M_y^2 \sim 1.1$ using the definition of M^2 . We found that as we increased the device current to 2.4 A, there was no significant change in M^2 in either the x or y direction. No beam steering over the entire current range was observed, and it is clear from the figure that relatively little change in the near- or far-field width occurs as the cw current is increased to 2.4 A. Taking the output power into consideration, we estimate that the average brightness of the 915-nm SCOWL beam at a current of 2.4 A is ~ 89 MW/cm²-str. We achieved similar brightness levels for our 980-nm devices. This average brightness level is higher than generally measured for conventional broad-area devices [9].

Thus, with appropriate facet passivation and coating of 1-cm-long devices, we have extended the cw output power of the 915-nm SCOWL device to >1 W. By measuring the beam quality of the SCOWL, we have shown that $M_x^2 \sim M_y^2 \sim 1.1$ over the entire range of output powers measured, and the average brightness is $\sim 89 \text{ MW/cm}^2\text{-str}$.

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3. SUBMICROMETER TECHNOLOGY

3.1. SUBMICROSECOND, SUBMILLIWATT, SILICON-ON-INSULATOR THERMO-OPTIC SWITCH

Silicon-on-insulator (SOI) is an attractive material system for the fabrication of photonic integrated circuits and optoelectronic devices at the 1.55- μm wavelength. The inherent high-index contrast between Si and SiO_2 strongly confines the optical energy, permitting sharp waveguide bends to ultrasmall devices. Spector et al. [1] have reported operational 1-m-long waveguides on 0.25- cm^2 chips. SOI technology has the inherent advantage that the single-crystal Si layer used for the waveguides is also available for complementary metal-oxide semiconductor (CMOS) transistor drivers and detectors. An SOI optical switch, as reported here, is an important component for an optical-CMOS integrated circuit.

Previously reported thermal Mach-Zehnder interferometer optical switches have been made with SiO_2 [2], Si_3N_4 [3], polymers [4], and Si [5]–[7]. SiO_2 and Si_3N_4 based switches require 100 and 300 mW of power and switch in 100 μs to 10 ms, while polymer and Si devices require 10–100 mW of power and switch in 3–100 μs . Here, we discuss a new approach where Si waveguides are directly heated by passing current through them. These devices have a thermal time constant of 500 ns with a required switching power of 5.5 mW. Switching power can be further reduced to <100 μW by heating both arms of a Mach-Zehnder switch.

Standard integrated circuit processing was used to form the thermal switches: lithography, reactive ion etching, ion implantation, and annealing. Si waveguides $0.26 \times 0.4 \mu\text{m}$ on a side and isolated from the silicon substrate by 1 μm of thermal SiO_2 were used to form the switches. Selected regions of the waveguide were made conductive by ion implantation doping with boron to $1 \times 10^{18} \text{ cm}^{-3}$, and electrical contacts were made to the waveguide with Si waveguide stubs connecting the primary waveguide to the Al contact pads. The stubs were designed to isolate the metal contacts, which are optically lossy, from the main optical path. Details of fabrication are reported elsewhere [8]. Figure 3-1 shows one of several fabricated switch designs, and Figure 3-2 shows the electrical contacts to the waveguide.

When heating only one arm of the Mach Zehnder switch, 5.5 mW is required to switch between maximum and minimum transmission, as shown by Figure 3-3. This power produces a temperature difference between the arms of 36°C. Devices were operated with a temperature difference of ~300°C for hours without any detrimental effects. As the voltage across the heated region of the Si waveguide is increased, an electric field appears between the Si substrate and the waveguide. This field causes free carriers to move from the biased contact into the undoped regions of the waveguide outside of the Mach-Zehnder switch. The reduction in transmitted power with increasing heater power is the result of absorption by these free carriers.

By heating both arms of the switch with a bias voltage, $\pm V_{\text{bias}}$, as in Figure 3-4(a), the power (applied to the signal lead) required to switch from minimum to maximum transmission, P , can be significantly reduced and is given by

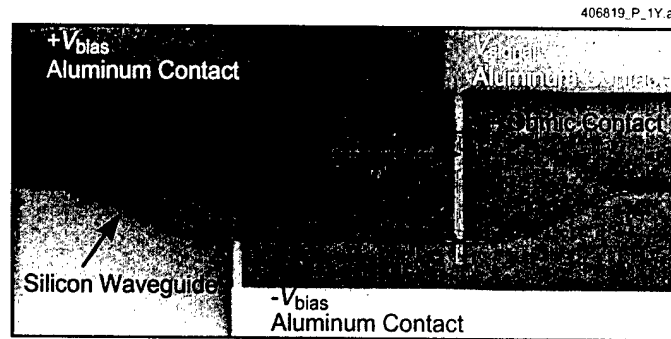


Figure 3-1. Scanning electron micrograph (SEM) of thermal Mach-Zehnder switch formed in Si waveguide. The device is 200 μm long and 50 μm wide. The heated region is 115 μm long. The top left and bottom Al contact pads are for biasing, and the upper right Al contact pad is for the signal input.

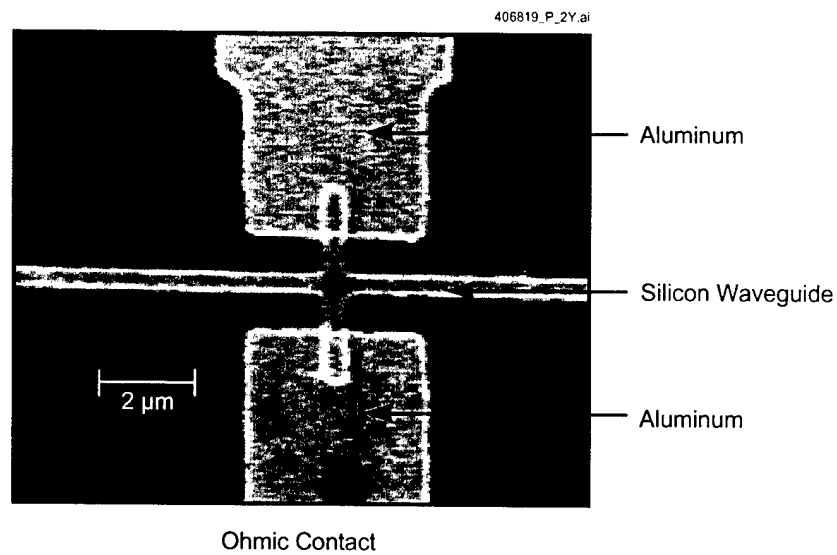


Figure 3-2. SEM of electrical contact to the Si waveguide. All contacts are symmetric about the waveguide to avoid exciting lossy asymmetric modes.

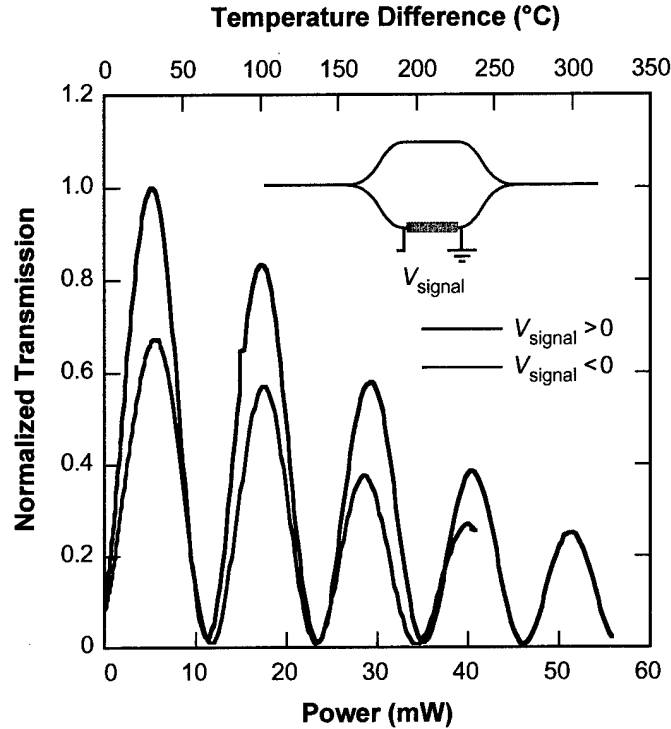


Figure 3-3. Transmitted 1.5- μm radiation as a function of power dissipated in one arm of a Mach-Zehnder switch. The heated region is 115 μm long. The temperature difference between the arms is shown on the top axis, and the applied power is indicated on the bottom axis. The inset depicts the Mach-Zehnder switch with only one arm heated.

$$\frac{P_{\pi}}{P_S} = \frac{P_S}{16P_{\text{bias}}} \quad (3.1)$$

where P_S is the power to switch using only one arm (5.5 mW) and P_{bias} is the bias power generated by $\pm V_{\text{bias}}$ when $V_{\text{signal}} = 0$. It is assumed that for $V_{\text{signal}} = 0$, no current flows through the signal terminal and that the optical transmission is midway between minimum and maximum transmission, i.e., quadrature. Switching powers $P < 100 \mu\text{W}$ have been experimentally obtained.

To demonstrate switching speed, the interferometer shown in Figure 3-4(a) was biased for maximum transmission at $V_{\text{signal}} = 0$, with $\pm V_{\text{bias}} \sim 100 \text{ V}$. This arrangement is experimentally simpler than the quadrature biasing described above. The switching time between 10 and 90% transmission is $\sim 600 \text{ ns}$, as shown in Figure 3-4(b). This is in agreement with small-signal measurement of the thermal time constant, 500 ns. The switching power was $P = 0.5 \text{ mW}$ and $P_{\text{bias}} = 20 \text{ mW}$.

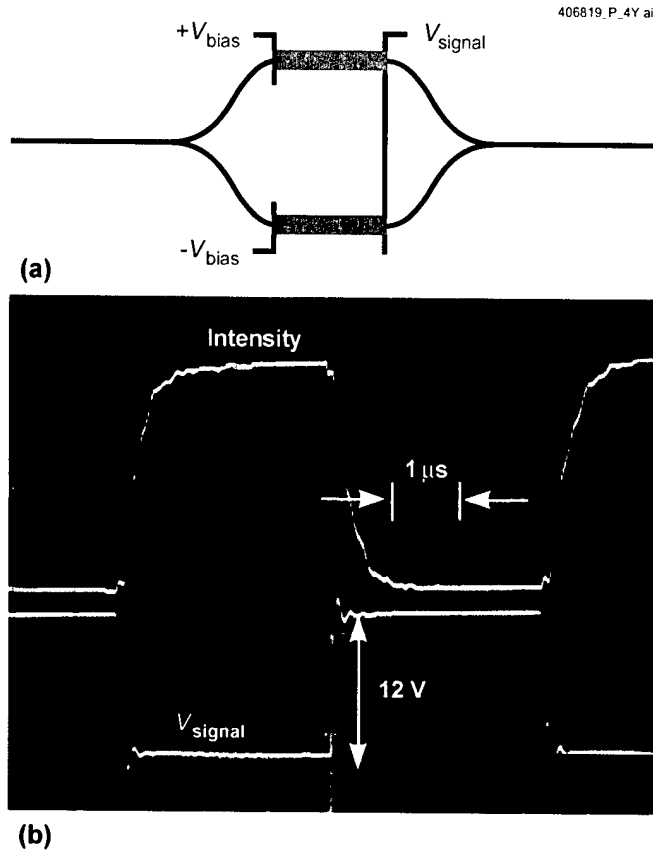


Figure 3-4. (a) Schematic drawing of the bias and input connections to a Mach-Zehnder switch. The heated regions are both $115\ \mu\text{m}$ long and are driven differentially. (b) Optical switching characteristic. The top curve is the transmitted light intensity, which is switched from maximum to minimum transmission, and the bottom curve is the input voltage signal, which is switched from 0 to 12 V.

Optical loss in waveguides similar to those used here is $\sim 7\ \text{dB cm}^{-1}$ [1],[9], loss to free-carrier absorption in the doped region is $\sim 10\ \text{dB cm}^{-1}$ [10], and the loss per electrical contact is $\sim 1\ \text{dB}$ for the electric field in the plane of the substrate and $\sim 1.5\ \text{dB}$ for the electric field out of the plane. Thus, for a $200\text{-}\mu\text{m}$ -long switch the loss is 2.5 dB, primarily from the electrical contacts.

This is the first report of a thermal Mach-Zehnder switch with directly heated waveguides having a switching time $< 1\ \mu\text{s}$ and a switching power of 0.1 to 5.5 mW. This device is also one of the smallest reported thermal Mach-Zehnder switches, $200 \times 50\ \mu\text{m}$. By heating both arms of the switch with a bias voltage, the switching power can be significantly reduced to $< 100\ \mu\text{W}$. Although the driving voltages used for this demonstration are from 10 to 100 V, these voltages can be significantly reduced to $< 10\ \text{V}$ by using $10^{19}\ \text{cm}^{-3}$ *n*-type doping, passivating the Si waveguides with thermal oxide to improve carrier mobility,

and using more electrical contacts to the waveguide. This SOI technology allows for both CMOS circuitry and optical waveguides.

We believe switching times can be reduced to <100 ns by pulsing the input signal voltage above that required for switching of a short time [11],[12].

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3.2 HYBRID MULTIMODE/SINGLE-MODE WAVEGUIDES FOR LOW LOSS

Strip waveguides are a promising architecture for integrated photonics devices. The high-effective-index contrast of strip waveguides results in compact photonics devices, permitting many devices, such as switches [5],[13] and wavelength filters [14], to be fabricated in a small space. However, the high-effective-index contrast also causes a large amount of light to scatter from any waveguide roughness, leading to a large propagation loss. Such losses limit the utility of strip waveguide devices and, in particular, make applications that inherently need long propagation paths, such as tunable true time delay [15],[16], impossible. One method for lowering such losses is to create much smoother sidewalls by oxidizing silicon strip waveguides [17]. We have obtained excellent results from this method and achieved losses of 2–3 dB/cm. To further lower the loss, we have invented a technique to exploit the lower-loss properties of wide waveguides without incurring any negative effects from their inherent multimode behavior. An order of magnitude reduction in loss was achieved.

It is well known that losses can be lowered in a strip waveguide by making the waveguide wider [17]. However, a waveguide cannot be made very wide before it supports the propagation of higher-order modes. The presence of higher-order modes is undesirable because it leads to dispersion and to unpredictable behavior in devices that rely on interference. In the hybrid method described here, a single-mode waveguide is coupled by a taper to a multimode waveguide, as shown in Figure 3-5, exciting only the fundamental mode in the multimode region. Although the multimode region can support higher-order modes, as long as the waveguide is straight and free of defects the fundamental mode will propagate without exciting higher-order modes. Another taper is used to connect back to a single-mode waveguide for turns or to couple to other devices. Defects and roughness do excite higher modes, but these modes cannot propagate in the single-mode waveguide sections and therefore merely cause a loss.

A two-dimensional simulation, using BeamPROP from RSI, shows that the loss in such a hybrid waveguide is expected to be significantly less than a simple single-mode waveguide. The simulation was run with $0.3\text{-}\mu\text{m}$ -wide single-mode regions and a $1.5\text{-}\mu\text{m}$ -wide multimode region. The length of the multimode region was $3000\text{ }\mu\text{m}$, the length of the tapers was $90\text{ }\mu\text{m}$, and the length of the single-mode regions was 60 and $180\text{ }\mu\text{m}$ at the beginning and end of the structure, respectively. The simulated roughness had a correlation length of 50 nm and an rms value of 2 nm. The loss predicted by the simulation

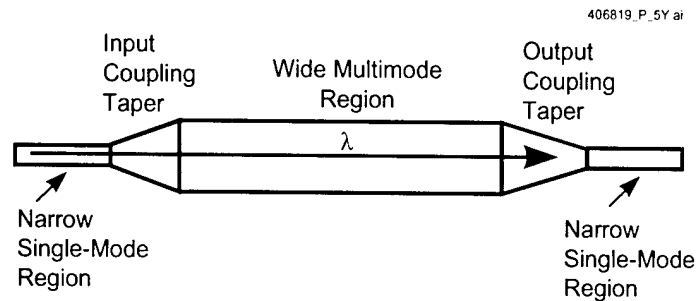


Figure 3-5. Sketch of hybrid waveguide method viewed top-down, illustrating transitions from single-mode to multimode regions.

was 8.0 dB/cm in the simple single-mode waveguide and 0.7 dB/cm in the hybrid structure, showing an order of magnitude improvement with the hybrid structure. Although these parameters do not exactly match the experiment below, the amount of improvement is expected to be qualitatively consistent with experimental results.

To test the method, devices were fabricated in single-crystal silicon on oxide. Starting material was UNIBOND SOI wafers purchased from Soitech with 1.5 μm of silicon on 2.0 μm of oxide. It was necessary to thin the silicon to 0.5 μm (by oxidation and wet etch) before doing optical lithography and a dry etch to define the waveguides. The single-mode regions were patterned 0.8 μm wide and the multimode regions 5.0 μm wide in this step. A wet oxidation at 1100°C was performed to smooth and shrink the waveguides. After the oxidation step the silicon in the single-mode region was 0.45 μm wide by 0.21 μm thick, and in the multimode region was 4.7 μm wide by 0.35 μm thick. The oxide created during the oxidation step is left on the waveguide and serves as its cladding. Figure 3-6 shows a cross section of the single-mode region. Three types of test features were fabricated: straight paths for Fabry-Perot measurements, paper clip paths, and long paths. This technique is polarization sensitive, and all measurements were made for the TE (in-plane) polarization. In the Fabry-Perot measurements a straight waveguide forms the cavity of a Fabry-Perot interferometer and the cleaved facets form the reflective surfaces. The fringe intensity can be used to determine the loss present in the waveguide [18]. In addition, dispersion or multiple paths in the cavity would be expected to lead to multiple frequencies or fringes. Figure 3-7 shows the Fabry-Perot fringes from a hybrid structure with 8 mm of multimode waveguide and 3 mm of total single-mode waveguide. The fringes are very regular, indicating that dispersion is low and that there is not a significant reflection at the tapers. A series of similar measurements were made to determine the loss of the different waveguide regions, which was determined to be 2.5 ± 0.5 dB/cm in the single-mode regions and 0.5 ± 0.5 dB/cm in the multimode regions. (Slightly better single-mode results of 1.9 ± 0.5 dB/cm were achieved in an earlier sample with a slightly wider, 0.55- μm -wide waveguide.)

The paper clip structures provide a more straightforward approach to measuring loss. These structures contain increasing amounts of either single-mode or multimode straight waveguide within an

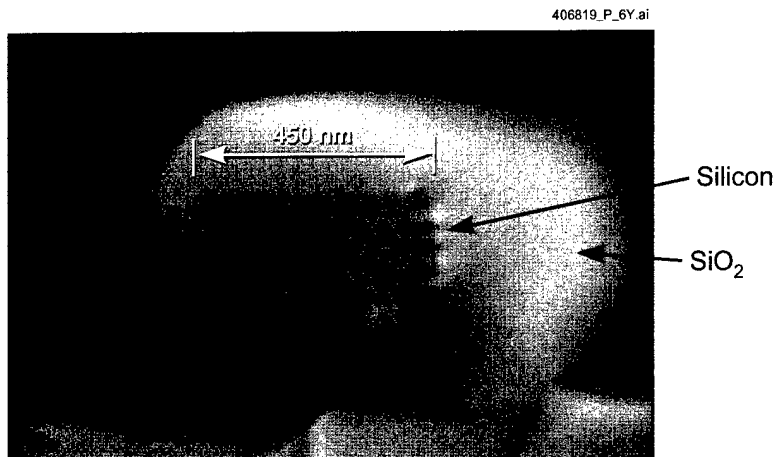


Figure 3-6. SEM cross section of single-mode waveguide region. The rectangle core material is silicon, and the cladding is silicon dioxide.

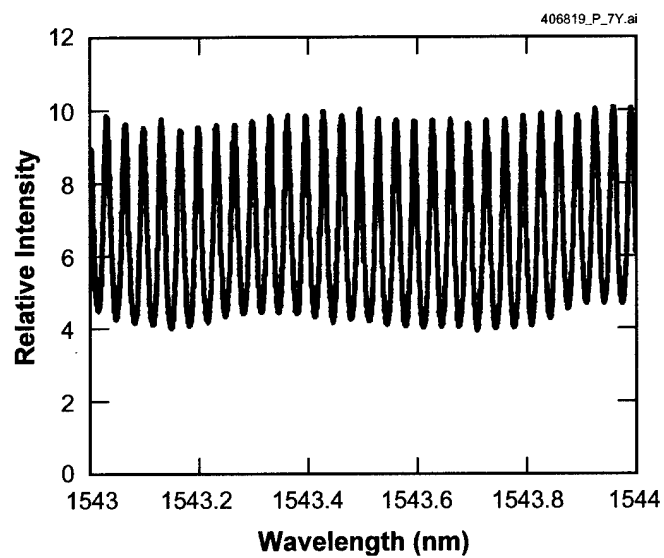


Figure 3-7. Fabry-Perot fringes from hybrid waveguide structure.

otherwise identical single-mode, snaking path. The difference in attenuation can therefore be entirely attributed to the difference in straight path length. The losses measured by this method are 2.9 ± 0.2 dB/cm and 0.18 ± 0.05 dB/cm for the single-mode and multimode regions, respectively. This measurement agrees with the value calculated from the Fabry-Perot measurements and shows the expected order-of-magnitude improvement of the multimode waveguides over the narrow waveguides.

To demonstrate the loss reduction that can be achieved in a system where both types of waveguides are combined, long snaking paths were fabricated. These paths mostly consisted of multimode regions, except for the turns, which were single-mode regions. The structures are illustrated in Figure 3-8. To

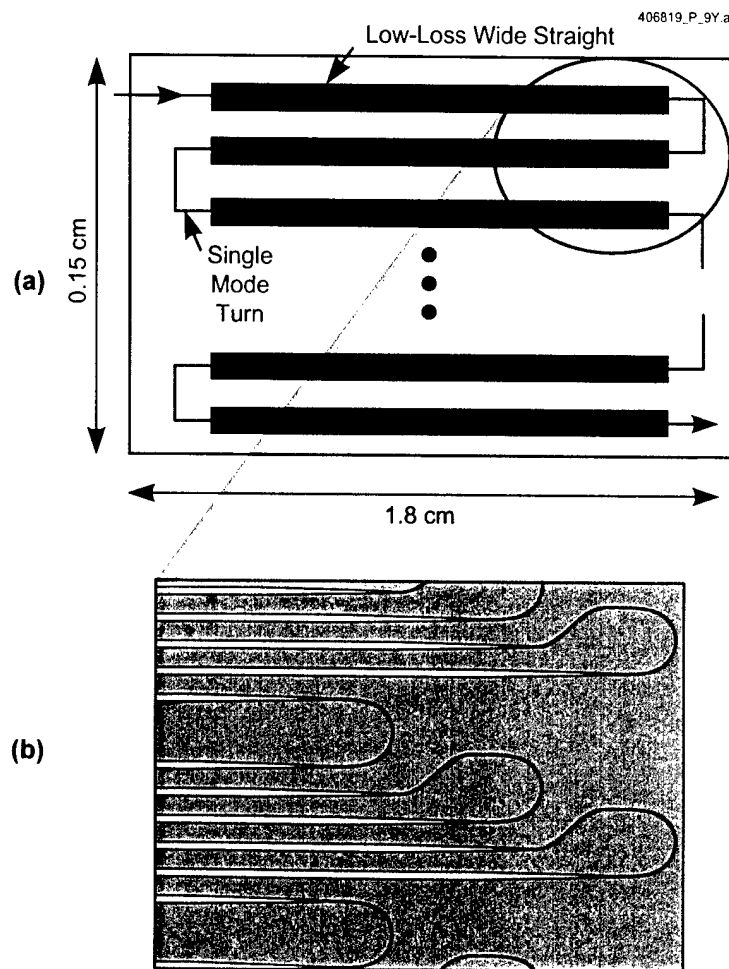


Figure 3-8. (a) Schematic drawing of 1-m-long serpentine delay line structure. The horizontal segments are wide multimode waveguides, and the curved segments are single mode. (b) Optical micrograph of one area of the waveguide showing the straight and curved segments.

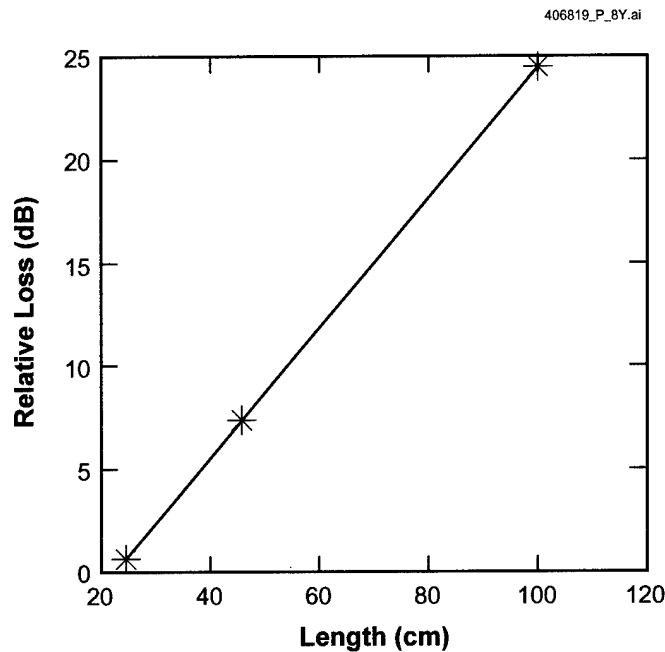


Figure 3-9. Experimental loss vs length for long hybrid waveguides. The slope of the fitted curve indicates an average loss of 0.32 dB/cm.

achieve maximum benefit the wide straight paths were fairly long at 1.73 cm. Three total lengths of 22, 44, and 101 cm were measured. Figure 3-9 is a graph plotting the relative transmission through the three different paths. A net loss of 0.32 ± 0.05 dB/cm is measured for the hybrid structure.

We have developed and demonstrated a novel and simple technique for achieving lower loss in any high-index waveguide system. Without using this novel technique we achieved losses of 2–3 dB/cm in silicon strip waveguides smoothed by oxidation. We believe this is the lowest result reported for a strip waveguide where the mode is not significantly expanded. By applying a further technique in which the waveguide is widened in the straight paths, the loss achieved was improved an order of magnitude to approximately 0.3 dB/cm. With this low loss, it was possible to get light through an unprecedented 1 m of silicon occupying an area of only 18×1.5 mm.

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4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 CANARY B-CELL SENSOR TECHNOLOGY FOR PATHOGENS IN FOOD

A CANARY (Cellular Analysis and Notification of Antigen Risks and Yields) B-cell line has been engineered to identify *Escherichia coli* O157:H7 with sensitivity and speed comparable to our other cell lines that recognize bacteria and large viruses. The performance of the CANARY assay with three sponsor-chosen food samples was determined, first with a bacterial simulant and then with *E. coli* O157:H7 after the cell engineering was accomplished. Sample preparation techniques have been developed that allow a desirable limit of detection and false-positive rate with all three foods.

In developing this B-cell line, genes were cloned from a cell line producing an antibody specific for *E. coli* enterohemorrhagic strains O157:H7 and O26:H11 (ATCC, HB-10452). The genes were inserted into expression vectors, and the completed vectors were used to create a stably transfected B-cell line. This B-cell line responds specifically to *E. coli* O157:H7, either live or formaldehyde-inactivated, but not to a nonpathogenic strain of *E. coli*. The sensitivity of the cell line is comparable to all cell lines developed to date that are specific for organisms large enough to be concentrated in a microcentrifuge, demonstrating a limit of detection of 50 colony-forming units (cfu) in a laboratory sample, as seen in Figure 4-1.

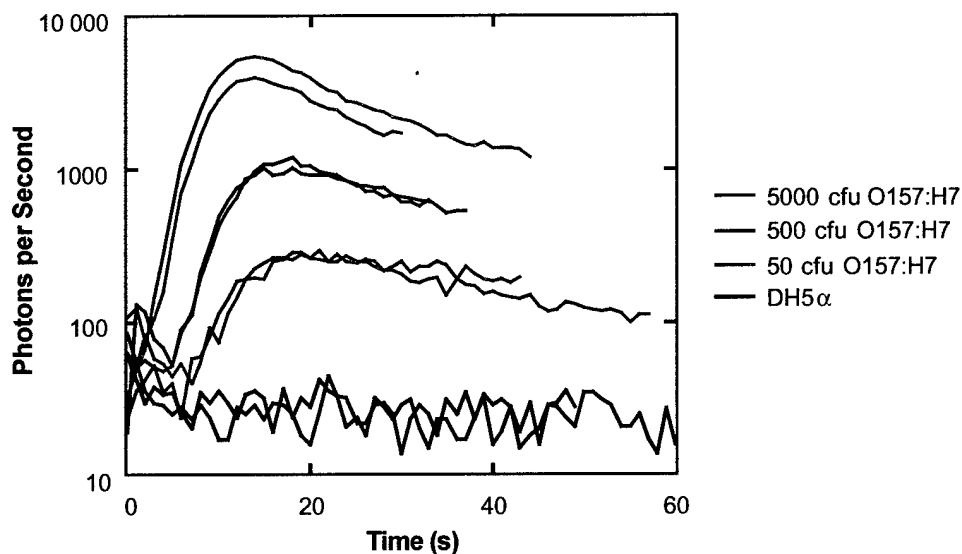


Figure 4-1. Detection of *Escherichia coli* O157:H7 compared with another strain of *E. coli* (DH5α). B cells specific for *E. coli* O157:H7 respond to as little as 50 cfu of that strain but not to DH5α.

In order to analyze CANARY performance with complex matrices, food samples with added bacterial simulant, *Yersinia pestis*, were processed with a stomacher. While multiple inhibitors were observed, several could be removed by the filtration and replacement method. This involves passing the sample through a 5- μ m syringe filter, concentrating the bacteria with centrifugation, and replacing the liquid with CANARY assay medium. However, the limit of detection was still restricted to 2×10^6 cfu/g with apple, 1×10^4 cfu/g with lettuce, and 2×10^4 cfu/g with pineapple, because of the presence of inhibitors that could not easily be separated from the bacteria. Therefore, alternative methods of recovering bacteria from food samples were investigated.

A technique that rinses the exterior of the sample, which is the most likely location to be contaminated, was investigated to determine if it would allow adequate recovery of bacteria but reduce the effect of inhibitors released from the food. Food samples with added *E. coli* O157:H7 were subjected to vigorous shaking with extraction medium, and the liquid was processed by the filtration and replacement method, as described for the stomached samples. The procedure is outlined in Figure 4-2. Because this method avoids the release of inhibitors that occurs when food is pulverized, we are able to demonstrate detection of as little as 500–1000 cfu of *E. coli* O157:H7 per gram in 25-g samples of lettuce, apple, and pineapple, as seen in Figure 4-3 and Table 4-1. Additionally, the entire assay takes only 5 min, including the time required for the preparation of the sample.

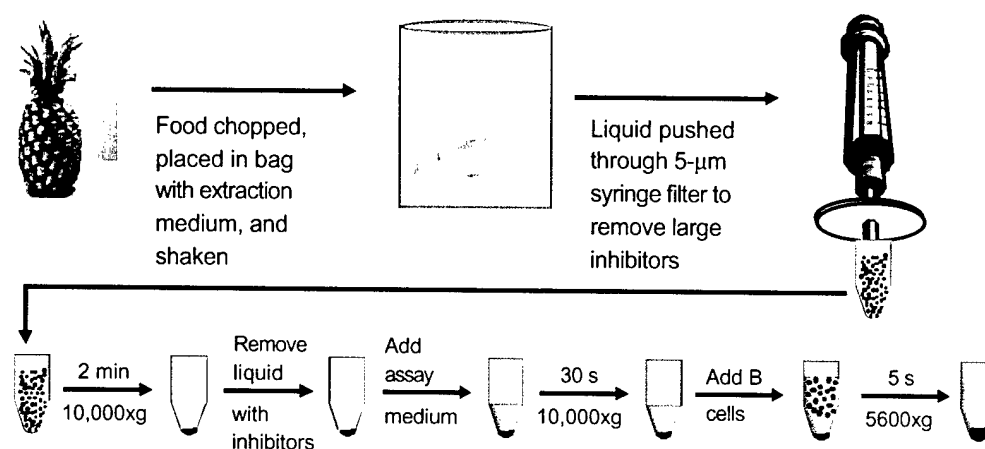


Figure 4-2. Sample preparation of food for the CANARY assay. 25-g samples were placed in a stomacher bag, *E. coli* O157:H7 was placed on the surface of the food, extraction medium was added, and the sample was shaken vigorously. The liquid was removed and passed through a 5- μ m syringe filter. 1 mL of filtrate was centrifuged for 2 min at 10,000 rpm in a swing-bucket microcentrifuge, the supernatant was removed by aspiration and replaced with 200 μ L of assay medium, and the sample was centrifuged an additional 30 s. B cells were added to the sample and delivered to the bottom of the sample tube with a 5-s spin in the centrifuge luminometer.

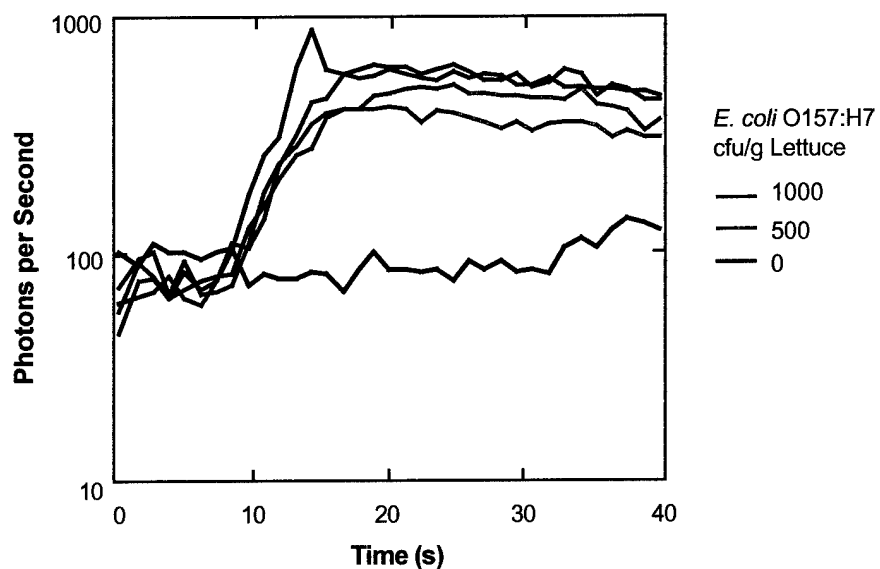


Figure 4-3. Detection of *E. coli* O157:H7 in food samples. 25 g of lettuce, with and without *E. coli* O157:H7, was processed as described in Figure 4-2, and the sample was tested with CANARY cells that respond to that pathogen. Similar results were obtained for apple and pineapple.

TABLE 4-1
Detection of *E. coli* in 25-g Food Samples*

Food	Volume (mL)	Positive/Total Tests	
		500 cfu <i>E. coli</i> per gram	1000 cfu <i>E. coli</i> per gram
Pineapple	10	13/21 = 62%	14/17 = 82%
Apple	10	18/20 = 90%	18/18
Lettuce	20	20/20	21/21
*The sample preparation method is presented in Figure 4-2. Each preparation was tested in duplicate.			

The assays of food samples were continued in the presence and absence of *E. coli* O157:H7 over a period of weeks in order to determine the probability of detection at low inoculations and the false-positive rate for the CANARY assay. As seen in Table 4-1, detection of 500 cfu/g of the pathogenic *E. coli* was observed 100% of the time in lettuce, 90% of the time in apple, and 62% of the time in pineapple. The probability of detection of 1000 cfu/g increases to 100% for apple and 82% for pineapple. The false-positive rate of 0.4% (1 in 251 tests) for all food types processed in this manner is identical to that observed for clean laboratory samples.

Thus, the CANARY assay has been shown to be compatible with food samples. Simple, rapid sample preparation techniques were developed that reduce the effect of inhibitors present in three food types. The entire assay takes only 5 min, including the time required to prepare the food sample.

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M. S. Petrovick

5. ADVANCED IMAGING TECHNOLOGY

5.1 DEVELOPMENT OF LOW-DARK-CURRENT PHOTODIODES WITH FDSOI-CMOS BACKEND METALLIZATION

A number of ongoing complementary metal-oxide semiconductor (CMOS) based imager programs have involved the development of sensitive back-illuminated photodiode arrays. These arrays will be attached to low-noise CMOS readout circuitry using either indium bump bonding techniques or, alternatively, three-dimensional integration techniques: wafer-to-wafer bonding plus via etch and tungsten fill of fully depleted silicon-on-insulator (FDSOI)-CMOS layers [1]. The three-dimensional integration approach has stringent requirements for surface planarity of the diode metal contact pad for both the wafer bonding and subsequent through-via metal interconnect processes. The yield for the bump-bonded hybrid approach would likely be improved as well by development of a highly planar landing pad for the bump contact. A photodiode process is described here that uses very-large-scale-integration backend-metal techniques resulting in a planar surface for bonding, and low dark current and high quantum efficiency for sensitivity.

Figure 5-1 shows a scanning electron micrograph (SEM) of the cross section of an $8\text{-}\mu\text{m}$ p^+ -on- n^- photodiode fabricated on a high-resistivity ($>3000\ \Omega\text{-cm}$, n -type) Si substrate. The backend process consists of the following process steps. First, a thick oxide layer is deposited and planarized to $0.8\text{-}\mu\text{m}$ thickness. Next, $0.5\text{-}\mu\text{m}$ vias are formed in the oxide by plasma etching down to the Si surface. The vias

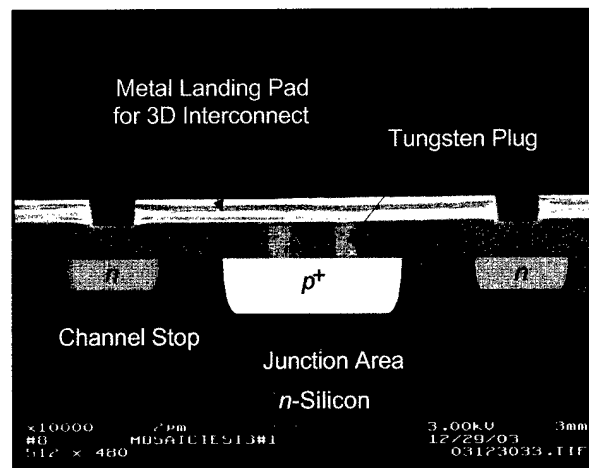


Figure 5-1. Scanning electron micrograph (SEM) cross section of an $8\text{-}\mu\text{m}$ diode fabricated using the fully depleted silicon-on-insulator (FDSOI) complementary metal-oxide semiconductor (CMOS) backend-metal process. Highly doped regions are highlighted.

are subsequently coated with a thin Ti/TiN adhesion layer and filled with a chemical-vapor-deposited tungsten metal. The wafer surface is then planarized again to remove excess surface tungsten above the plugs. A final Ti/AlSi/TiN metallization contact pad is formed by sputter deposition and subsequent dry etching. Then, subsequent to the final metallization, an H₂ anneal is done to reduce dry-etched induced damage from the backend process. The backend process consists of two dry-etching steps in contrast to our low-dark-current photodiode process previously reported [2], where we employed wet-chemical etching for both metal and oxide in order to avoid dry-etched induced damage that is known to increase dark current in diodes.

The measured dark current (from 0- to 10-V reverse bias) is displayed in Figure 5-2 for interconnected arrays of 24- μm (10,000) and 8- μm (90,000) diodes fabricated on the same wafer using the backend-metal process described above. Both arrays have the same total area ($5.76 \times 10^{-2} \text{ cm}^2$). The measurement technique has been described previously [2]. Both the 24- and 8- μm diode arrays show impressively low dark currents of 12 pA ($\sim 208 \text{ pA per cm}^2$) and 19 pA ($\sim 330 \text{ pA per cm}^2$), respectively. These results were obtained using our standard H₂ anneal subsequent to final metallization, and they indicate that any dry-etched induced damage from the backend process was adequately mitigated by the anneal.

The dark current data for the 8- μm array shown in Figure 5-2 exhibits anomalous behavior (compared to the 24- μm array) for reverse biases $> 3.6 \text{ V}$, where the current decreases slightly with increasing reverse bias. Note that the data also exhibit much less noise (above 3.6 V), even at these low

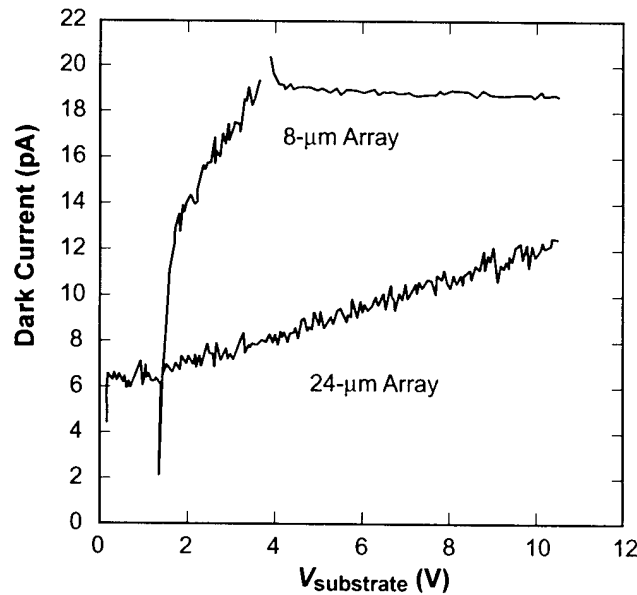


Figure 5-2. Measured dark current for arrays of 24- μm (10,000) and 8- μm (90,000) diodes from 0- to 10-V reverse bias.

current levels. Our previous work on pin diodes [2] indicates that surface state emission from the low-doped region at the Si surface between the more heavily doped channel-stop and junction regions of the device, shown in Figure 5-1, is the dominant source of dark current leakage for these arrays. For the 8- μm diode we used a metal contact pad, also shown in Figure 5-1, that overlaps this low-doped region of the device. When the diode is reverse biased, by positive bias applied to the substrate, the n -type surface becomes inverted by minority carriers. This inversion layer screens the surface states, suppressing the dark current in a manner identical to the effect observed in MOS-gated diode measurements and where noise associated with surface state emission may also be reduced. As the bias is increased, the extent of inversion layer encroachment increases into the lighter-doped portion of the channel-stop region resulting in a slight decrease in the dark current. For the 24- μm diode the metal contact pad does not extend past the junction edge into the low-doped region; thus, this effect is not observed.

Table 5-1 summarizes the dark current measurements made on a number of diode array wafers fabricated utilizing the FDSOI-CMOS backend-metallization process. Also included in Table 5-1 are the results obtained for two wafers fabricated using our standard wet-etch process, one a control wafer fabricated with the group 2A dry-etched photodiodes and the other a “best” wafer taken from a previously processed lot. Two wafers had both 8- and 24- μm diode arrays while the other four contained only 16- μm diode arrays. All wafers exhibited diode dark currents in the sub-nA/cm² range. The model used to predict the dark current is based on surface state generation currents of ~ 1 nA/cm² coming from the low-doped surface region (between channel stop and junction) plus bulk current contributions of ~ 50 pA/cm² and has been described elsewhere [2]. Measured results are usually somewhat higher than predicted by the model; however, the inversion layer surface-clamping effect described above, exhibited by wafer 1, results in smaller dark current than predicted (for the 8- μm array only). Backend process wafers 2A-4 and 2A-5, however, exhibit very low dark currents, much lower than wafer 2A-1 (the wet-etched “control” wafer) and even somewhat better than the “best” wet-etched results.

The accuracy of the model used to predict the dark current depends critically on the estimate of the extent of the depleted surface area between the junction and channel-stop regions under reverse bias conditions. Because the dominant source of diode capacitance comes also from the channel-stop/junction regions, there is an inverse relationship between diode capacitance and dark current. If the channel-stop/junction separation is small, diode capacitance is high and leakage is low, while the reverse is true for large separations. Thus, the diode capacitance can be used to estimate diode leakage. Figure 5-3 shows the calculated diode capacitance per micrometer for an 8- μm diode array for three channel-stop/junction combinations: standard process, standard process plus long anneal, and high channel-stop implant dose plus long anneal. It was initially believed that the dark current could be lowered merely by using the standard process and annealing the wafer longer to bring the channel-stop and junction regions closer together and also raising the capacitance. From the capacitance data, initially at low bias the capacitance is indeed higher; however, as the reverse bias increases the capacitance actually becomes smaller compared to the standard process, indicating that the depletion region extent (effective channel-stop/junction separation) is greater for the long-anneal wafer. The 10–15% lower capacitance for the long-anneal wafer should result in higher dark current, which indeed is observed for wafer 2A-5 compared to 2A-4, as seen in

TABLE 5-1
Photodiode Dark Current Measurement Summary

		8- μ m Pixel			16- μ m Pixel		24- μ m Pixel	
Wafer No.	Channel Stop/ Junction	Measured (pA/cm ²)	Model (pA/cm ²)	Inversion Clamp (V)	Measured (pA/cm ²)	Model (pA/cm ²)	Measured (pA/cm ²)	Model (pA/cm ²)
CMOS Backend Metal Process								
1	Standard Process	330 620*	440	3.6	-	-	210	160
5	High Dose + Long Anneal	555 580*	400	9.2	-	-	190	145
2A-4	Standard Process	-	-	-	170-185	220	-	-
2A-5	High Dose + Long Anneal	-	-	-	215-240	240	-	-
Wet Process Diodes								
2A-1	Standard Process	-	-	-	625-800	220	-	-
6	Standard Process	-	-	-	225	220	-	-
*Estimated without inversion clamping.								

Table 5-1. In order to lower the dark current, the dose of the channel-stop implant should be increased, as shown by the results of Figure 5-3. This accounts for the improvement of dark current observed for both the 24- and 8- μ m arrays (without inversion clamping) of wafer 5 compared to wafer 1.

A number of diode arrays incorporating the FDSOI-CMOS backend-metal process that are fully compatible with three-dimensional wafer integration techniques have been fabricated, and the dark current has been measured. The results appear very encouraging where values comparable to or better than our previous low-dark-current diode arrays, fabricated using conventional wet-etch processing, have been obtained.

D. D. Rathman D. J. Young

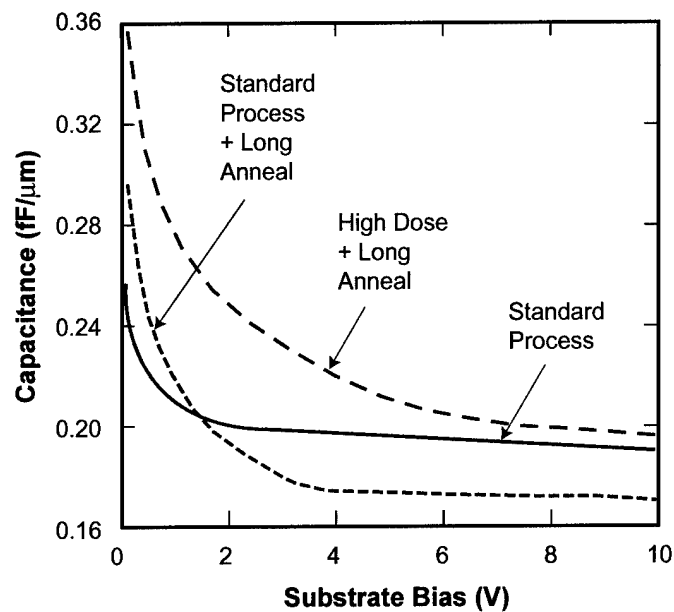


Figure 5-3. Simulated capacitance per micrometer width for three channel-stop/junction implant/anneal combinations: standard process, standard process plus long anneal, and high dose (2× standard channel-stop implant dose) plus long anneal.

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6. ANALOG DEVICE TECHNOLOGY

6.1 DEMONSTRATION OF CHARGE-COUPLED DEVICES IN A FDSOI PROCESS

Previously, we reported the development of very low power, moderately high speed analog-to-digital converters based on charge-coupled device (CCD) technology [1]. In an effort to further reduce power consumption and to extend conversion rates into the gigahertz range, the possibility of implementing CCDs in our fully depleted silicon-on-insulator (FDSOI) technology has been investigated. Here, we report what we believe is the first definitive demonstration of an FDSOI CCD. Our initial circuit-test results are presented, and a new fabrication process (which could also be applied to conventional, non-SOI devices) is described. The process allows an array of CCD gates to be fabricated within a single layer of polycrystalline silicon (polysilicon) by forming well-controlled, very narrow gaps in the polysilicon layer. While FDSOI CCDs retain the high linearity and charge storage density of surface-channel CCDs, the buried-oxide layer allows strong fringing electric fields to penetrate beneath the gates and accelerate the transfer of charge from gate to gate.

Because CCDs had not previously been demonstrated in FDSOI and because the process for forming narrow gaps was new, we designed the initial test chip to explore a wide range of design parameters. In addition to process-test structures and test transistors, there were many variations of CCD shift register design. Some CCDs were designed for relatively low speed testing with a conventional probe card; others were designed for high-speed testing with microwave probes. All of the CCDs were based on a very simple design that required the smallest number of applied signals. They used three clock phases. It should be noted that most conventional CCDs, being implemented with two overlapping polysilicon layers, used a four-phase design so that all gates of a given phase would be in the same layer of polysilicon. All of the gates in our process, however, are formed from a single polysilicon layer, so we could use a three-phase design. The voltage-to-charge sampler at the input and the charge-to-voltage readout circuit at the output used the same clock signals as the rest of the CCD. Thus, only five ac signals are required: three clock phases, the input signal, and the output signal. Figure 6-1 illustrates the topology of the CCDs and the steps in the clock sequence that perform input sampling and output readout and reset.

Various parameter spaces were explored in the test chip. CCDs were laid out with nominal (target) gap widths from 0 to 200 nm in steps of 10 nm. Those values were based on an oversimplified model of the process in which the physical gaps would be 200 nm smaller than the gaps drawn on the mask, which ranged from 200 to 400 nm. The actual gaps were expected to deviate from the nominal values. The narrowest gaps were nearly certain to be shorted, and the widest gaps were nearly certain to leave potential barriers between the gates during CCD operation that would prevent efficient charge transfer. In addition, since we did not know how good or poor the charge-transfer efficiency might be in FDSOI silicon, CCDs were laid out with 1, 2, 5, 10, 20, 50, 100, and 200 stages. The shortest shift register, with only one stage, was likely to work as long as the process successfully formed CCDs. The longest shift register, with 200 stages, is long enough to measure transfer losses sufficiently small to support the implementation of a

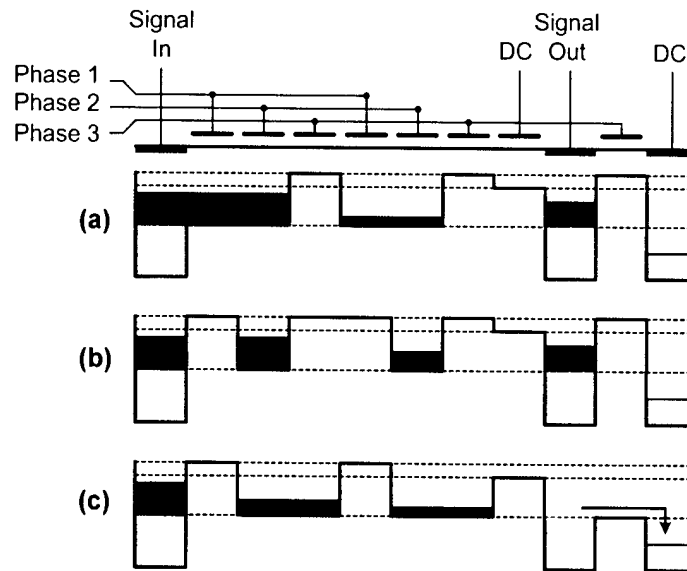
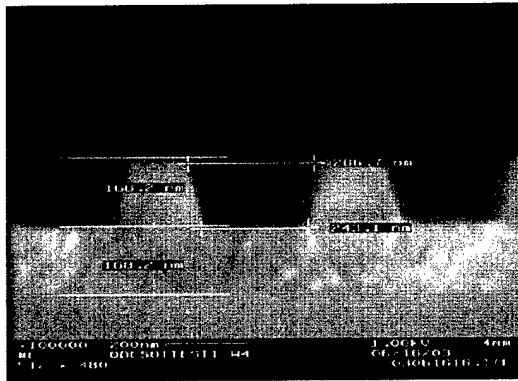


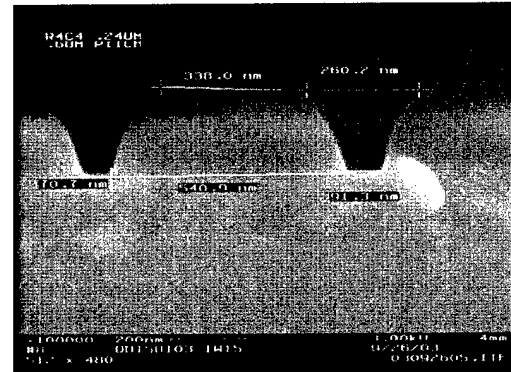
Figure 6-1. Diagram of layout topology and operation of a two-stage, three-phase charge-coupled device (CCD). The top part of the drawing shows the arrangement and wiring of the gates and diffusions. The drawing below shows how the charge is distributed at various times. (a) Phases 1 and 2 are on, allowing the signal on the input diffusion to create a charge packet under those gates that follows the input signal. Meanwhile, phase 3 has turned off, forcing a charge packet into the floating-diffusion sensor (signal out), which is connected to an on-chip source follower amplifier (not shown). (b) Phase 1 has just turned off, isolating a new input sample under phase 2. (c) Phase 3 has turned on. It does double duty as the reset gate, restoring a reference level on the floating diffusion.

charge-domain analog-to-digital converter. Finally, CCDs were laid out with gate-to-gate pitches of 400, 500, 600, 700, 800, 900, 1000, 1200, and 1500 nm. The shortest gates would transfer charge the fastest and thus would operate up to the highest clock frequencies, perhaps at speeds beyond what we could test. Therefore, we included CCDs with gates much longer than we would expect to use in real circuits but where dynamic loss of charge-transfer efficiency would set in at a much lower frequency.

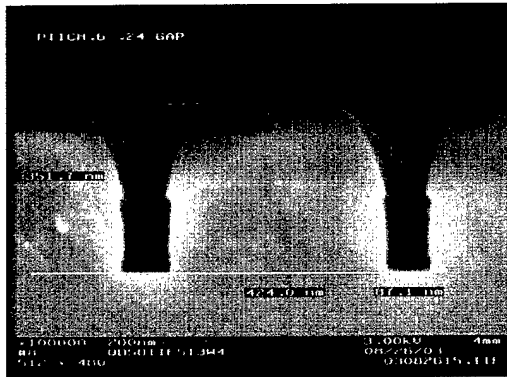
In the fabrication process the gaps that are created in the polysilicon gate layer have dimensions much smaller than the smallest lithographic feature supported. The sequence of steps, illustrated by the scanning electron micrographs (SEMs) in Figure 6-2, begins with a continuous 200-nm-thick layer of polysilicon on top of a 4.2-nm gate oxide in the areas that will become CCDs. A 200-nm layer of TEOS (tetra-ethyl-ortho-silicate) oxide is deposited and patterned with openings that are nominally 200 nm wider than the final gaps. Figure 6-2(a) shows a pattern with gaps of ~240 nm between oxide strips ~160 nm wide (gate pitch of 400 nm). Then, an additional 100 nm of TEOS oxide is deposited and etched, without using a mask, to form a nominally 100-nm-thick spacer around the original TEOS pattern. This reduces the width of the original openings by 200 nm (nominally). The SEM in Figure 6-2(b) shows an opening ~90 nm wide at the bottom and 260 nm wide at the top. The resulting oxide layer serves as a hard mask



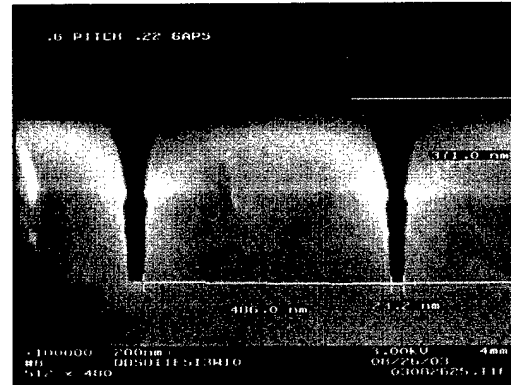
(a)



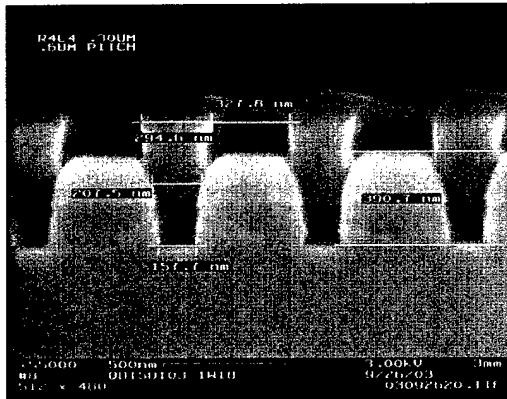
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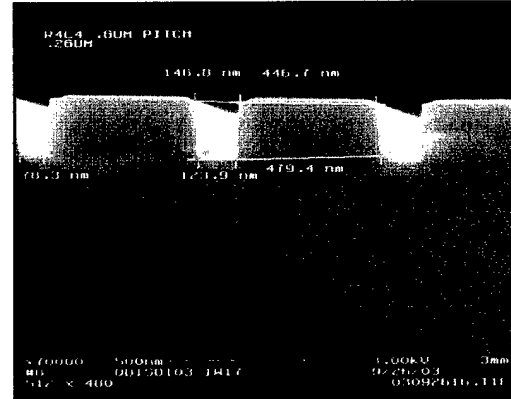
(c)



(d)



(e)



(f)

Figure 6-2. Scanning electron micrograph (SEM) showing steps in fabrication of gaps in the polysilicon gate layer, which can be much smaller than dimensions defined lithographically. For example, (d) shows a gap <25 nm.

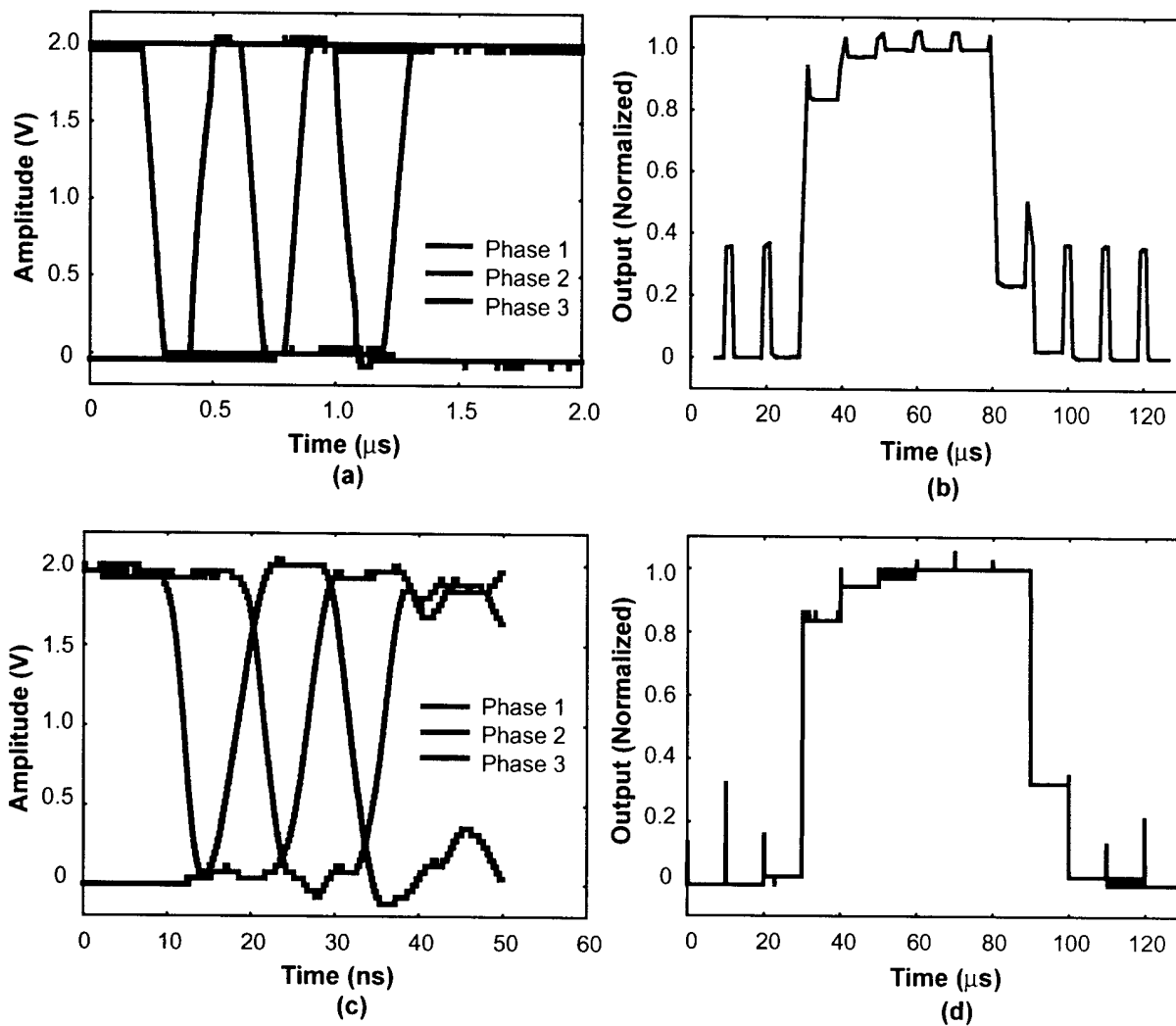


Figure 6-3. Clock waveforms and corresponding output signals from a 200-stage CCD operated at two different effective clock frequencies, showing (a),(b) a sequence of transitions over 900 ns at a repetition rate of one sequence per 10 μs , and (c),(d) a sequence shortened to 30 ns at the same repetition rate. Charge-transfer losses are seen in output signals that do not immediately reflect their full value after a sharp transition in the input signal. The first output charge packet that should be at 100% is only at about 83%. The first output at a falling edge is 76% and 68% of the way down with the slow and fast clock waveforms, respectively.

for a highly anisotropic etch of the polysilicon, with the results shown in Figure 6-2(c), where the resulting gap in the polysilicon is ~90 nm. Figure 6-2(d) shows another CCD structure where the final gap is only 23 nm. Now comes the most challenging step: removing the thick oxide hard mask without attacking the very thin gate oxide exposed in the gaps. This is done by protecting the gaps with photoresist while etching the hard-mask oxide, as shown in Figure 6-2(e). When the resist is removed, the CCD gate structure is complete, with very narrow gaps in a single layer of polysilicon, as shown in Figure 6-2(f).

The results from two tests of CCD circuits, at effective clock speeds differing by a factor of 30, are shown in Figure 6-3. The clock waveforms used to operate the CCDs are shown on the left and the corresponding output signal waveforms on the right. The input signal was a sequence of pulses, and we verified that the output pulses emerged after delays corresponding to the number of stages in the CCDs, which for the examples shown is 200.

The clocks were operated in a burst mode. Each clock phase was held at a static level—phases 1 and 2 high, phase 3 low, as in Figure 6-1(a)—during most of the 10- μ s repetition period. During that static interval the output signal is valid and can be observed clearly, without interference from clock feedthrough. In addition, the input signal has that entire interval available to make its transition from one value to another. The six-step clock burst sequence begins with phase 1 going low, which captures a sample of the input signal, as seen in Figure 6-1(b). As seen in Figure 6-1(c), phase 3 then goes high, dumping the charge in the output sensing circuit and resetting the output diffusion to a reference level. The narrow pulses in the output signals in Figure 6-3 at each 10- μ s multiple correspond to the time when phase 3 is on. Those pulses actually go to a constant level above the top of the output plots, but filtering in the plotting software has reduced their apparent amplitudes.

With perfect charge transfer in the CCD, the rising edge of the output pulse would reach the full amplitude immediately. The observed level of about 80% of the full amplitude corresponds to 0.1% of the charge being left behind with each complete clock cycle. Subsequent samples pick up charge left behind from the previous sample that exactly compensates for the charge they left behind. When the signal falls, the level does not reach zero immediately because of the accumulated charge left behind by the previous large signal. The output waveforms in Figure 6-3 exhibit a slight asymmetry between the rising and falling edges, indicating that the charge-transfer inefficiency depends to some extent on the size of the charge packet.

Simulations of CCDs in FDSOI indicate that they should be able to transfer charge fast enough to support clock speeds into the gigahertz range. We are currently setting up experiments to operate the CCDs at much higher speeds than shown in Figure 6-3.

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7. ADVANCED SILICON TECHNOLOGY

7.1 LARGE-TUNING-RANGE ANALOG AND MULTI-BIT MEMS VARACTORS

High-capacitance-ratio ($>80:1$) microelectromechanical series (MEMS) and shunt switches have been demonstrated from 0.1 to 100 GHz [1],[2] and have been employed in low-loss phase shifters. Low-capacitance-ratio ($<10:1$) and high-quality-factor MEMS varactors can enable new tunable and adaptive circuits such as matching networks, filters, and high-precision analog-to-digital converters. Several analog MEMS varactors with capacitance ratios of 1.2:1 to 3:1 have been demonstrated recently [3]–[5]. With analog MEMS varactors, biasing and control can be difficult because of nonlinearity and hysteresis. Digital-type (multi-state and multi-bit) varactors may help simplify the control and reduce nonlinear effects like self-biasing under rf power. Here, we present results of large-tuning-range analog varactors as well as multi-state and multi-bit varactors for tunable filter and matching network applications.

A variety of analog MEMS varactors were implemented using the MEMS switch technology developed at MIT Lincoln Laboratory. A typical analog MEMS varactor is shown in Figure 7-1. The buried pull-down electrode and the rf contact region are highlighted with false color to enhance the contrast of the scanning electron micrograph (SEM). The analog varactor is actuated by applying a voltage between the curled trilayer cantilever and one or both of the pull-down electrode and the rf output line. The rf contact region is made up of two fingers surrounded on three sides by the buried pull-down electrodes.

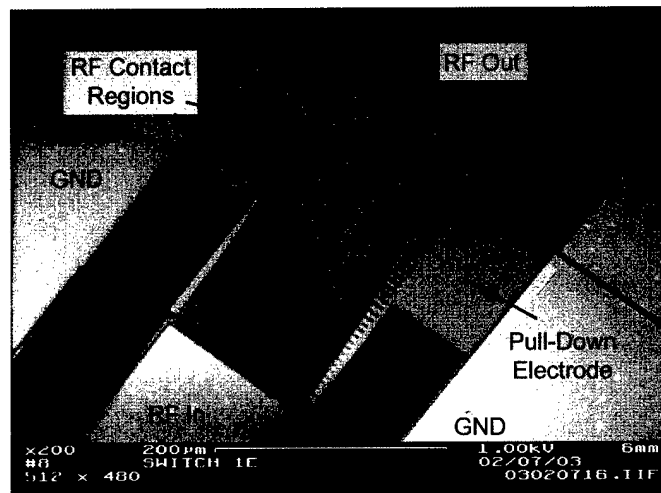


Figure 7-1. Scanning electron micrograph (SEM) of microelectromechanical series (MEMS) capacitive varactor. The resistive pull-down electrodes and the rf contact area are highlighted with false color.

When the varactor is actuated, the cantilever and the rf contact area form an overlap capacitance. The amount of overlap capacitance is controlled by adjusting the magnitude of the voltage between the cantilever and the pull-down electrode, V_1 , and the cantilever and the rf contact area, V_2 .

The design of these novel varactors makes use of a stress-controlled trilayer ($\text{SiO}_2/\text{Al}/\text{SiO}_2$) membrane as the switching element. The structures were designed and simulated using an iterative nonlinear-mechanical and electrostatic simulation tool. Thick dielectric layers over segmented pull-down electrodes and interdigitated air gaps formed by corrugations in the cantilever layer reduce the electric field intensity in the dielectrics and extend the lifetime of the switch [6].

The devices were fabricated in a Laboratory class 10 solid state complementary metal-oxide semiconductor (CMOS) fabrication facility. The MEMS process is fully compatible with the CMOS flow and can withstand temperatures above 350°C . The steps are illustrated in Figure 7-2. The devices are fabricated on high-resistivity silicon wafers coated with a 150-nm-thick thermal silicon dioxide layer. The buried high-resistance (50 k per square) TaN electrodes are sputtered and then patterned with a plasma etch process and then covered with 150 nm of plasma-enhanced chemical vapor deposited (PECVD) oxide. The first metal layer is evaporated and patterned with a lift-off process. The 600-nm-thick metal stack is coated with a thick PECVD oxide, which is subsequently made planar with a novel etch/chemical-mechanical-planarization process, leaving 50-nm-thick oxide over the metal stack and 700-nm-thick oxide over the buried electrode. The corrugation layer is a sputter-deposited inorganic layer and is patterned with a wet-chemistry etch. The wet etch is designed to create a 45° tapered sidewall to prevent the formation of cusps in subsequent layers. The release layer is a similarly deposited and patterned layer. The bottom layer of the trilayer membrane is a 100-nm-thick oxide deposited in a PECVD system, resulting in a net compressive residual stress. Vias are etched through the bottom oxide layer to allow for electrical contact between the first metal layer and the middle Al layer, which is sputter deposited and then covered by a 100-nm-thick PECVD oxide with low-compressive residual stress. The trilayer membrane is patterned and etched in a plasma etch system. The sacrificial layer is removed in a wet-chemistry process and can be released in a standard spin rinse dryer or a commercial CO_2 critical point dryer.

The S-parameters of the MEMS analog varactors were measured using an Agilent Precision Network Analyzer and a Cascade Summit 1200 probe station in room air. The switches were biased using a short-rise-time bipolar square-wave signal for the voltage between the cantilever and the pull-down electrode (V_1), and the cantilever and the rf contact area (V_2). By adjusting V_1 and V_2 , as shown in Figure 7-3, the amount of overlap capacitance can be varied. The measured isolation for various states is shown in Figure 7-4. The isolation and insertion loss were used to extract an equivalent lumped capacitance for each measured state. Ripple and occasional jumping in the isolation traces are due to the slight modulation of the varactor by the switching bipolar waveform. A plot of the extracted equivalent capacitance and impedance (at 10 GHz) vs voltage for another sample device is shown in Figure 7-5. A capacitance tuning range of nearly 1.5 decades was achieved as well as a nearly linear impedance variation vs voltage. This nearly linear impedance variation is important to tunable matching network circuits. It is seen that only the region of high capacitance exhibits hysteresis. The capacitance values for a given voltage were observed to be very repeatable. The slight modulation of the capacitance by the finite rise time of bipolar waveform for

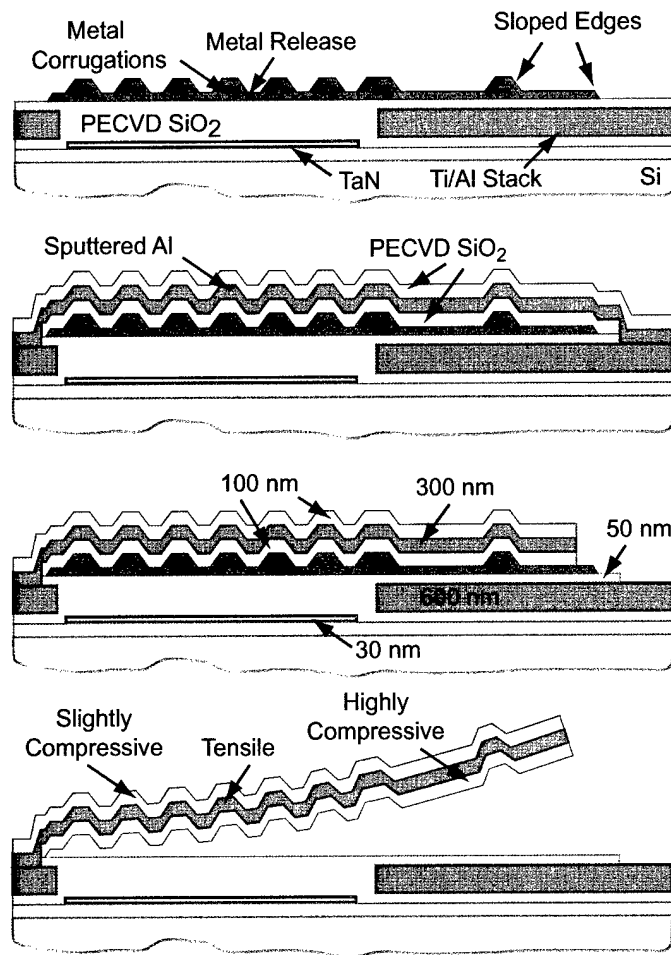


Figure 7-2. Illustration of MEMS fabrication flow. The fabrication steps are all complementary metal-oxide semiconductor (CMOS) compatible. Chemical-mechanical planarization and novel wet etches prevent sharp edges and subsequent cusps in overlying layers. Drawing not to scale.

this type of analog varactor is unavoidable unless the rise time is much shorter than the response time of the switch in a particular deformed state. For this reason we also developed multi-state and multi-bit devices that can be held in fixed contacting positions by multiple electrodes.

Some circuit topologies such as tunable filters and matching networks could benefit from varactor elements that can give increasing but small changes in coupling capacitance (5–20 fF), and some circuits would benefit from a device that can give small changes in coupling capacitance (10–30 fF) as well as several states with larger capacitance (300–1000 fF). To avoid the modulation seen in the analog varactor,

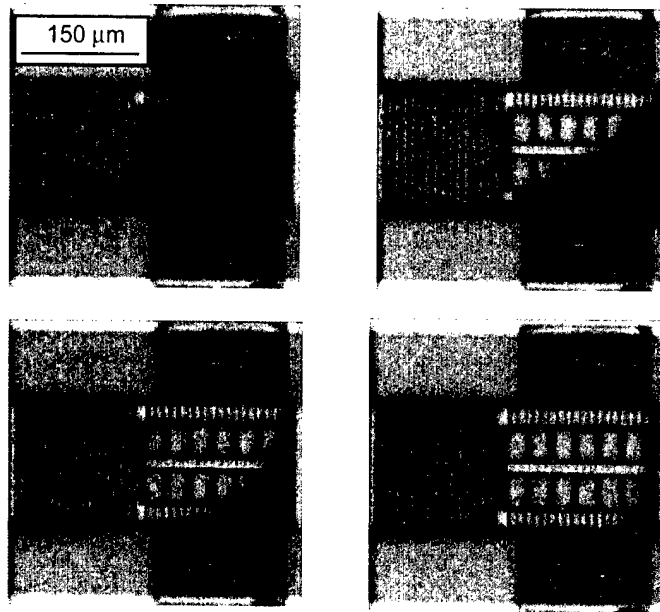


Figure 7-3. Optical micrographs of analog MEMS varactor shown with increasing areas of rf contact.

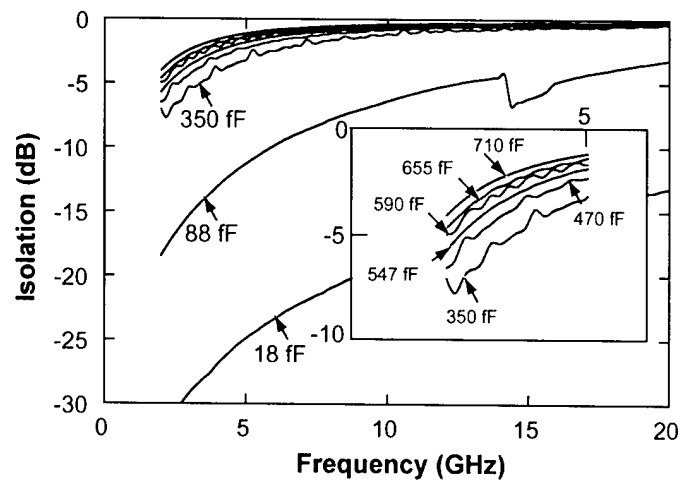


Figure 7-4. Measured insertion loss and fitted capacitance values for first-generation MEMS analog varactor.

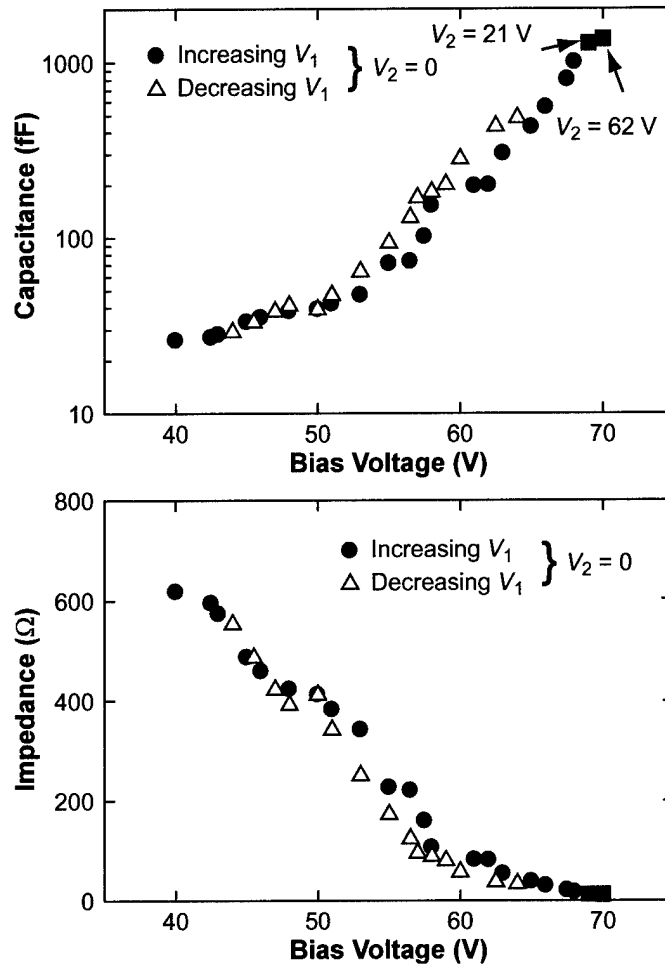


Figure 7-5. Extracted equivalent capacitance and impedance (at 10 GHz) vs voltage for typical MEMS analog varactor.

several multi-state varactor devices were designed and fabricated using multiple individually addressed pull-down electrodes. A coupling varactor developed for filter and tunable oscillator circuits is shown in Figure 7-6. The device has five buried pull-down electrodes, allowing for six different bias states and corresponding fringing capacitance values. The capacitance values as extracted from the measured isolation and insertion loss for the six states, seen in Figure 7-6, are 5.1, 7.6, 9.8, 11.1, 13.8, and 17.7 fF for states 0–5, respectively. These fixed-state capacitance values did not exhibit modulation because of the bipolar biasing waveform.

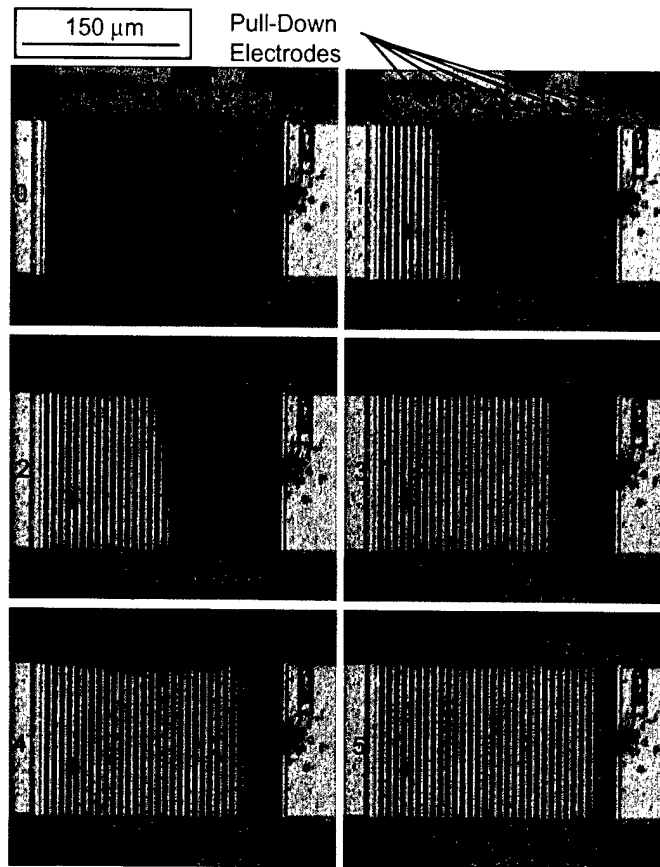


Figure 7-6. Photomicrographs of multi-state coupling varactor. The switch has five buried pull-down electrodes, allowing for six bias states with increasing fringing capacitance (5.1–17.7 fF).

Another multi-state varactor device designed to give small and large changes in capacitance is shown in Figure 7-7 in various fixed bias states. This device has three buried pull-down electrodes as well as the capacitive rf contact areas, which give five possible fixed bias states with capacitances of 8.8, 13, 23, 340, and 1009 fF for states 0–4, respectively.

The scalable nature of the Laboratory curling cantilever switch device and the extremely high capacitance ratio ($>100:1$) make it highly suited to multi-bit capacitor banks. The standard capacitive switch (with a down-state capacitance of 1.1 pF) is used as the third most significant bit in a 4-bit capacitor. Each switch has one half the capacitive overlap area of the switch representing the next significant bit, allowing for capacitance values from ~ 20 fF to 4.5 pF with a least significant bit value of 300 fF. The 4-bit capacitor is shown in Figure 7-8 in a sampling of the 16 possible states. The total device width is $540 \mu\text{m}$ and the length $260 \mu\text{m}$ and is implemented in a microstrip configuration. The overall size and number of

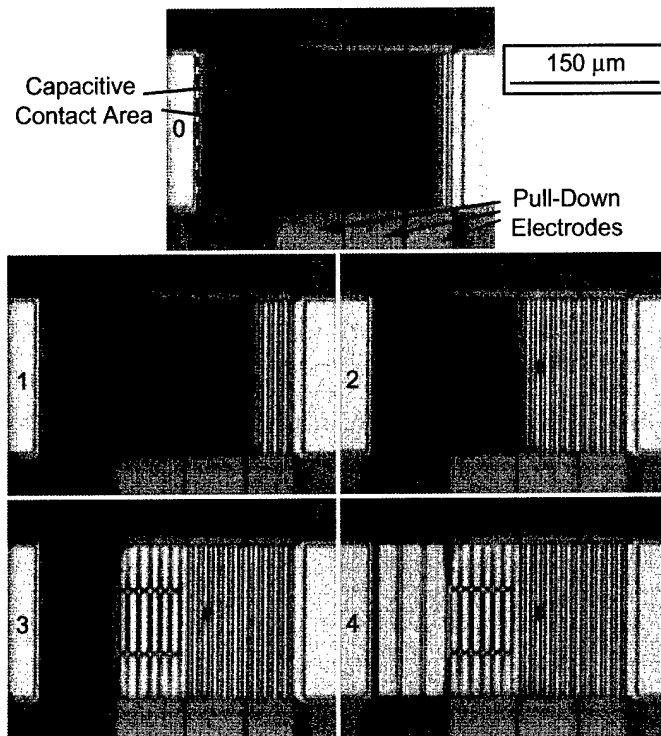


Figure 7-7. Photomicrographs of a multi-state varactor and switch. The varactor has three buried pull-down electrodes as well as capacitive rf contact areas that can give five possible bias states. States 0–2 have fringing capacitance only, and states 3–4 have parallel-plate capacitance, giving capacitances of 8.8, 13, 23, 340, and 1009 fF for states 0–4, respectively.

constituent devices can be reduced, for a given number of bits and maximum capacitance value, by combining appropriately sized multi-state varactors, described earlier. The 4-bit capacitor was designed to be tested on a thinned wafer with back-side vias for proper operation of the microstrip transmission lines. The devices reported here were tested on a full-thickness wafer without vias, making difficult the accurate extraction of the capacitance values from rf measurements of each state.

In conclusion, the Laboratory MEMS capacitive switch technology has been modified and enhanced to produce analog, multi-state, and multi-bit varactors for application in tunable filters, matching networks, and oscillators. Analog varactors were demonstrated with better than 1.5-decade tuning range. Multi-state varactors for coupling applications (5–20 fF) and tuning applications (8–1000 fF) were also demonstrated. Finally, a 4-bit capacitor bank was fabricated, providing a capacitance range from ~20 fF to 4.5 pF with a least significant bit value of 300 fF.

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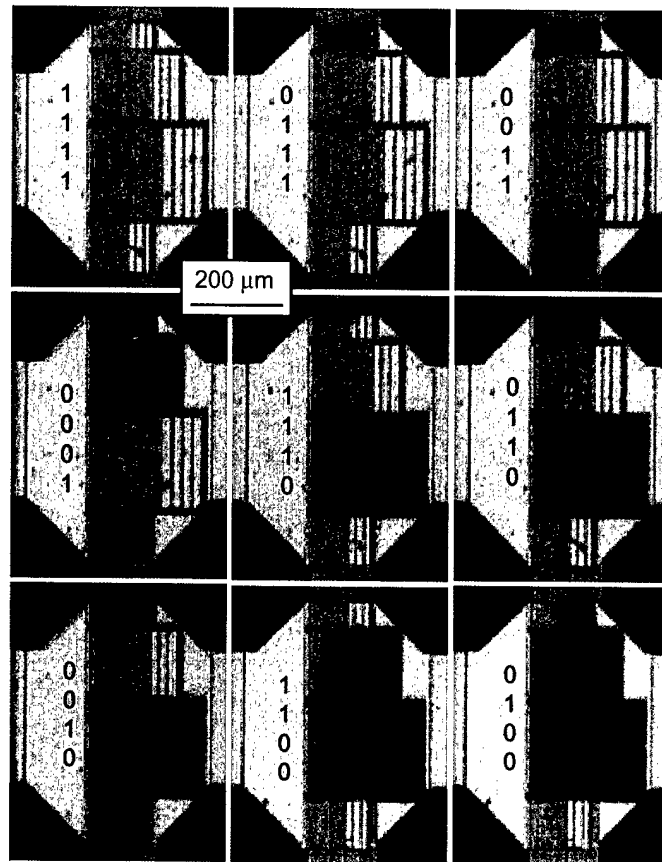


Figure 7-8. Photomicrographs of 4-bit capacitor in a sampling of biased states. The devices have capacitive contact areas that are one half the area of the next significant bit switch. The capacitance ranges from ~ 20 fF to 4.5 pF with a least significant bit value of 300 fF.

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